CONFIDENTIAL B

MT6358 Power Design Notice (Only for MT6771)

V1.1

2018/03/05

History

Revision	Date	Author	Description
V0.1	2017/09/14	Goto	Initial
V0.2	2017/10/14	Goto	1. P4 – Update Power plan. 2. P35 – Update temp information. 3. P64~65 – VPA Output Capacitance Notice. 4. P71 – Update LDO capacitor range. 5. P72~75 – Update layout constraint. 6. P80 – Update layout constraint for VIO_1V8
V0.3	2017/10/29	Goto	1. P5 – Update Buck Power Plan 2. P7 -- Update LDO Power Plan 3. P53, P61 -- Update DCDC 4. P72, P73, P75 – Update layout constraint
V1.0	2017/12/26	Goto	1. P4 – Update Power plan. 2. P13 – Update Power on/off Sequence. 3. P14 -- Update VXO22 Power On/Off Behavior 4. P53 – Update Output Decoupling. 5. P79 – Update Layout Constraint of VREF. 6. P82~P87 -- Add AP Analog Power PCB Layout Constrain. 7. P103~P118 – Add PCB Layout Guideline. 8. P119 -- Add How to Connection for Unused Pin
V1.0.1	2018/01/11	Goto	1. P4 -- Update Power plan. 2. P6, P14 -- Update VXO22 Iout_max and Power On/Off Behavior. 3. P13 -- Update VPROC12 off Sequence. 4. P106, P108, P110, P113, P114 -- PCB Layout Guideline 5. P65 – Update VPA Output Capacitance Notice.

History

Revision	Date	Author	Description
V1.1	2018/03/05	Goto	1. P5, P9, -- Update Power Plan : Update VIO18 to 700mA. 2. P17, P18 – Change the UVLO on With Charger in 3.0V. 3. P14 – Remove the note : Power off from RESETB to VUSB/VAUD28 : 2-3mS. 4. P63 – Add Remote Sense Application Notice: Layout Guide (4). 5. P74, P75 – Update the layout constraint of the L1 ≤ 7nF LDO. 6. P117 – HOMEKEY : Update short to GND if not used and check the long press function.

Content

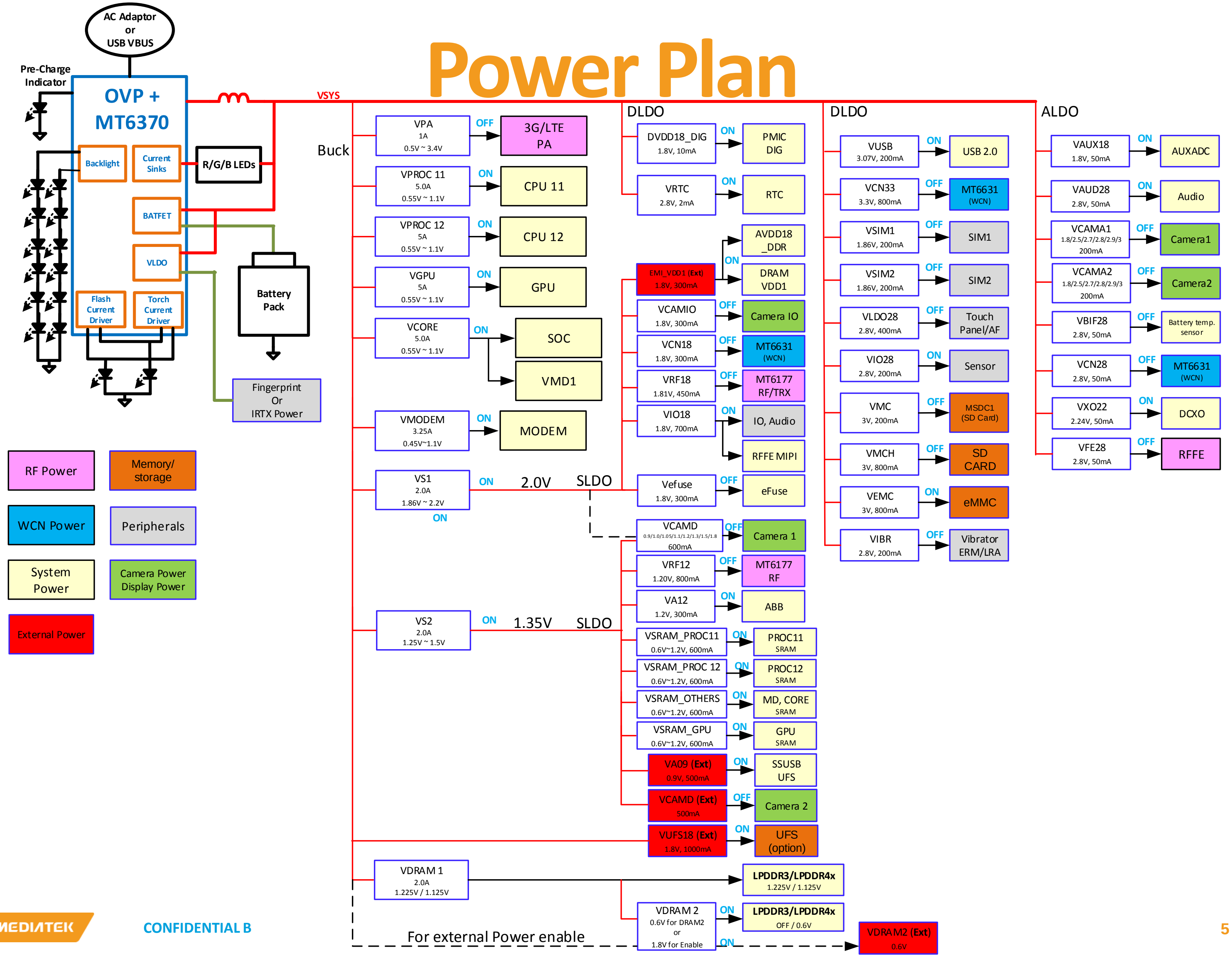
- **MT6358 Introduction**
- Function Description
- Reference Design
- Function Block Notice
- PCB Layout Guideline

MT6358 – General Description

- The MT6358 highly integrated function fulfill all power requirement in smart phone system
  - **Buck Converters**

    MT6358 x 9 (VPROC11, VPROC12, VCORE, VGPU, VMODEM, VDRAM1, VPA, VS1, VS2)
  - **LDOs**
    - Analog LDO * 8
    - Digital LDO * 23
    - RTC *1
  - **Driver**
    - Vibrator Driver *1
  - **Audio**
    - Audio Codec
    - Audio Line Out
  - **RTC Macro**
  - **Fuel Gauge**
  - **XO Control and Output**

Power Plan



AC Adaptor or USB VBUS
Pre-Charge Indicator
OVP + MT6370
Backlight
Current Sinks
R/G/B LEDs
BATFET
VLDO
Flash Current Driver
Torch Current Driver
Battery Pack
Fingerprint Or IRTX Power
VSYS
Buck
VPA 1A 0.5V ~ 3.4V
OFF
3G/LTE PA
VPROC 11 5.0A 0.55V ~ 1.1V
ON
CPU 11
VPROC 12 5A 0.55V ~ 1.1V
ON
CPU 12
VGPU 5A 0.55V ~ 1.1V
ON
GPU
VCORE 5.0A 0.55V ~ 1.1V
ON
SOC
VMD1
VMODEM 3.25A 0.45V~1.1V
ON
MODEM
VS1 2.0A 1.86V ~ 2.2V
ON
2.0V
SLDO
VS2 2.0A 1.25V ~ 1.5V
ON
1.35V
SLDO
VDRAM 1 2.0A 1.225V / 1.125V
LPDDR3/LPDDR4x 1.225V / 1.125V
VDRAM 2 0.6V for DRAM2 or 1.8V for Enable
ON
LPDDR3/LPDDR4x OFF / 0.6V
ON
VDRAM2 (Ext) 0.6V
For external Power enable
DLDO
DVDD18_DIG 1.8V, 10mA
ON
PMIC DIG
VRTC 2.8V, 2mA
ON
RTC
AVDD18 _DDR
ON
EMI_VDD1 (Ext) 1.8V, 300mA
DRAM VDD1
VCAMIO 1.8V, 300mA
OFF
Camera IO
VCN18 1.8V, 300mA
OFF
MT6631 (WCN)
VRF18 1.81V, 450mA
OFF
MT6177 RF/TRX
VIO18 1.8V, 700mA
ON
IO, Audio
RFFE MIPI
Vefuse 1.8V, 300mA
OFF
eFuse
VCAMD 0.9/1.0/1.05/1.1/1.2/1.3/1.5/1.8 600mA
OFF
Camera 1
VRF12 1.20V, 800mA
OFF
MT6177 RF
VA12 1.2V, 300mA
ON
ABB
VSRAM_PROC11 0.6V~1.2V, 600mA
ON
PROC11 SRAM
VSRAM_PROC 12 0.6V~1.2V, 600mA
ON
PROC12 SRAM
VSRAM_OTHERS 0.6V~1.2V, 600mA
ON
MD, CORE SRAM
VSRAM_GPU 0.6V~1.2V, 600mA
ON
GPU SRAM
VA09 (Ext) 0.9V, 500mA
ON
SSUSB UFS
VCAMD (Ext) 500mA
OFF
Camera 2
VUFS18 (Ext) 1.8V, 1000mA
ON
UFS (option)
DLDO
VUSB 3.07V, 200mA
ON
USB 2.0
VCN33 3.3V, 800mA
OFF
MT6631 (WCN)
VSIM1 1.86V, 200mA
OFF
SIM1
VSIM2 1.86V, 200mA
OFF
SIM2
VLDO28 2.8V, 400mA
OFF
Touch Panel/AF
VIO28 2.8V, 200mA
ON
Sensor
VMC 3V, 200mA
OFF
MSDC1 (SD Card)
VMCH 3V, 800mA
OFF
SD CARD
VEMC 3V, 800mA
ON
eMMC
VIBR 2.8V, 200mA
OFF
Vibrator ERM/LRA
ALDO
VAUX18 1.8V, 50mA
ON
AUXADC
VAUD28 2.8V, 50mA
ON
Audio
VCAMA1 1.8/2.5/2.7/2.8/2.9/3 200mA
OFF
Camera1
VCAMA2 1.8/2.5/2.7/2.8/2.9/3 200mA
OFF
Camera2
VBIF28 2.8V, 50mA
OFF
Battery temp. sensor
VCN28 2.8V, 50mA
OFF
MT6631 (WCN)
VXO22 2.24V, 50mA
ON
DCXO
VFE28 2.8V, 50mA
OFF
RFFE
RF Power
Memory/ storage
WCN Power
Peripherals
System Power
Camera Power Display Power
External Power

MT6358 Buck Power Plan

Circuit Type	Name	Output Voltage Range(V)	Default Voltage(V)	IOUT-Max(mA)	Expected use
BUCK	VPROC11	0.5 ~ 1.2 (6.25mV/step)	0.8	5000	PROCESSOR11
	VPROC12	0.5 ~ 1.2 (6.25mV/step)	0.8	5000	PROCESSOR12
	VGPU	0.5 ~ 1.1 (6.25mV/step)	0.8	5000	GPU
	VCORE	0.5 ~ 1.1 (6.25mV/step)	0.8	5000	Digital core always on
	VMODEM	0.5 ~ 1.29375 (6.25mV/step)	0.775	3250	MODEM
	VDRAM1	1.06 ~ 1.3 (12.5mV/step)	1.125/1.225	2000	DRAM
	VS1	1.86 ~ 2.2 (12.5mV/step)	2	2000	SYS LDOs Input
	VS2	1.25 ~ 1.5 (12.5mV/step)	1.35	2000	SYS LDOs Input
	VPA	0.5~3.4 (50mV/Step)	0.5	1000	3G/LTE PA

MT6358 LDO Power Plan (1)

Circuit Type	Name	Output Voltage (V)	IOUT-Max(mA)	Expected use
LDO	VFE28	2.8	50	RFFE
	VXO22	2.24	50	DCXO
	VRF18	1.81	450	RF
	VRF12	1.2	800	RF
	VEFUSE	1.71/**1.8**/1.84	300	EFUSE
	VCN33	3.3/3.4/**3.5**/3.6	800	Connectivity
	VCN28	2.8	50	Connectivity
	VCN18	1.8	300	Connectivity

MT6358 LDO Power Plan (2)

Circuit Type	Name	Output Voltage (V)	IOUT-Max(mA)	Expected use
LDO	VCAMA1	1.8/2.5/2.7/**2.8**/2.9/3.0	200	Camera Analog
	VCAMA2	1.8/2.5/2.7/**2.8**/2.9/3.0	200	Camera Analog
	VCAMD	0.9/1.0/1.05/1.1/**1.2** 1.3/1.5/1.8	600	Camera Digital Option to VA09 (SSUSB only) If VCAMD > 1.2, VS2_LDO4 connect to VS1, If VCAMD ≤ 1.2, VS2_LDO4 connect to VS2,
	VCAMIO	1.8	300	Camera IO
	VLDO28	**2.8**/3.0	400	CTP & Camera AF
	VA12	1.2	300	AP Analog Module
	VAUX18	1.8	50	AUXADC
	VAUD28	2.8	50	Audio
	VIO28	2.8	200	IO & Sensor

MT6358 LDO Power Plan (3)

Circuit Type	Name	Output Voltage (V)	IOUT-Max(mA)	Expected use
LDO	VIO18	1.8	700	IO & EMMC
	VSRAM_PROC11	0.6~1.2 (**0.9**)	600	SRAM_PROC11
	VSRAM_PROC12	0.6~1.2 (**0.9**)	600	SRAM_PROC12
	VSRAM_OTHERS	0.55~1.2 (**0.9**)	600	SRAM_OTHERS
	VSRAM_GPU	0.65~1.2 (**0.9**)	600	SRAM_GPU
	VDRAM2	**0.6**/1.8	600	LPDDR4x_VDDQ
	VMC	1.86/2.9/**3.0**/3.3	200	MSDC
	VMCH	2.9/**3.0**/3.3	800	SD Card
	VEMC	2.9/**3.0**/3.3	800	EMMC / UFS

MT6358 LDO Power Plan (4)

Circuit Type	Name	Output Voltage (V)	IOUT-Max(mA)	Expected use
LDO	VSIM1	1.7/1.8/**1.86**/2.76/3.0/3.1	200	SIM
	VSIM2	1.7/1.8/**1.86**/2.76/3.0/3.1	200	SIM
	VIBR	1.2/1.3/1.5/1.8/ 2.0/**2.8**/3.0/3.3	200	Vibrator
	VUSB	3.07	200	USB
	VBIF28	2.8	50	Battery Interface
	VRTC28	2.8	2	RTC
	DVDD18_DIG	1.8	10	PMIC Digital

Feature List

Function	MT6328	MT6353	MT6355	MT6356	MT6357	MT6358
Buck Converter	5	5	10	6	5	9
LDO	28	28	38	31	28	33
Driver	ISINK LED *2 ERM Vibrator *1	ISINK LED *2 ERM Vibrator *1	ERM Vibrator *1	ERM Vibrator *1	ISINK LED *1 ERM Vibrator *1	ERM Vibrator *1
Audio	Audio Codec Class-AB/D Amp x1	Audio Codec	Audio Codec	Audio Codec	Audio Codec	Audio Codec
Others	RTC macro	RTC macro	RTC macro	RTC macro	RTC macro	RTC macro SD_DET
Charger	1. Pulse Charger 2. Fuel Gauge	1. Pulse Charger 2. Fuel Gauge	Fuel Gauge	Fuel Gauge	1. Pulse Charger 2. Fuel Gauge	Fuel Gauge

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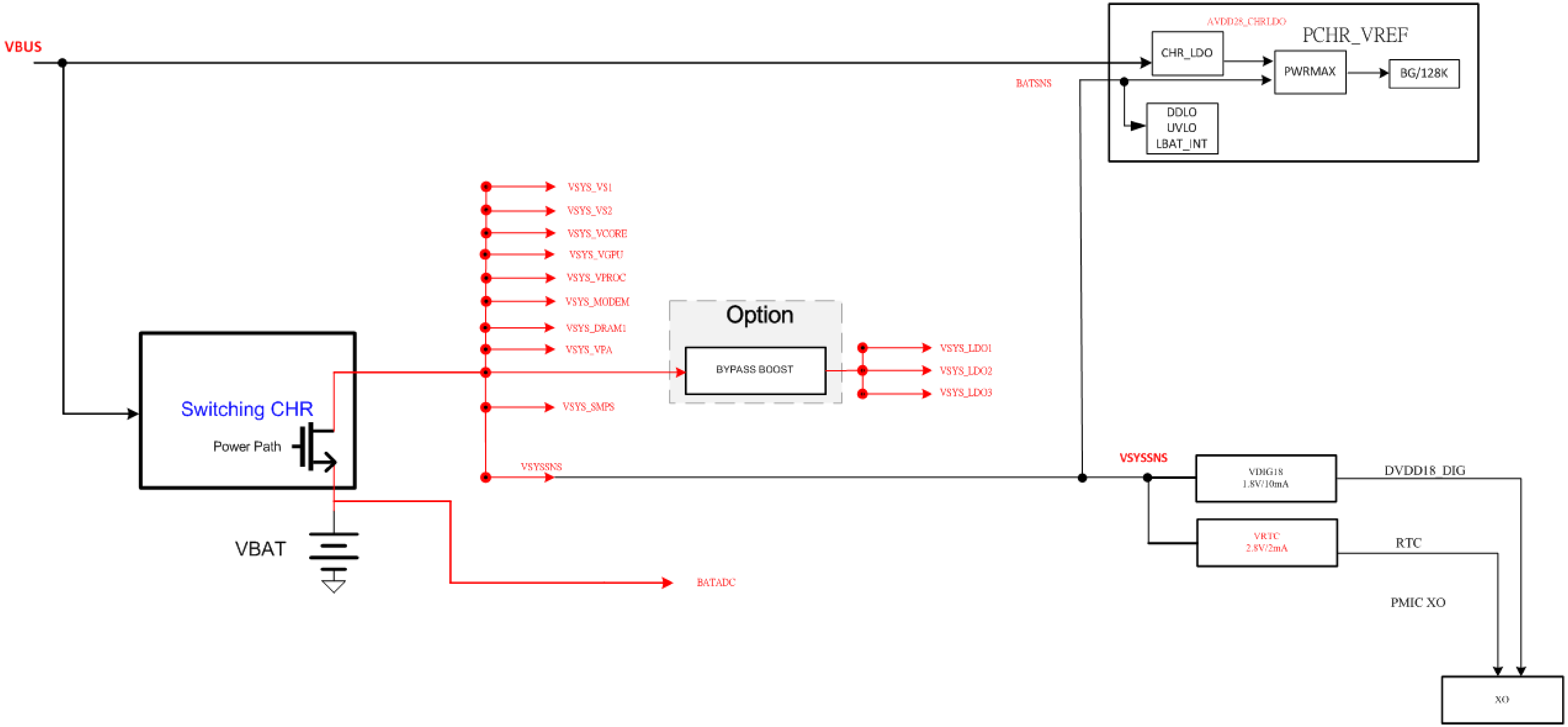
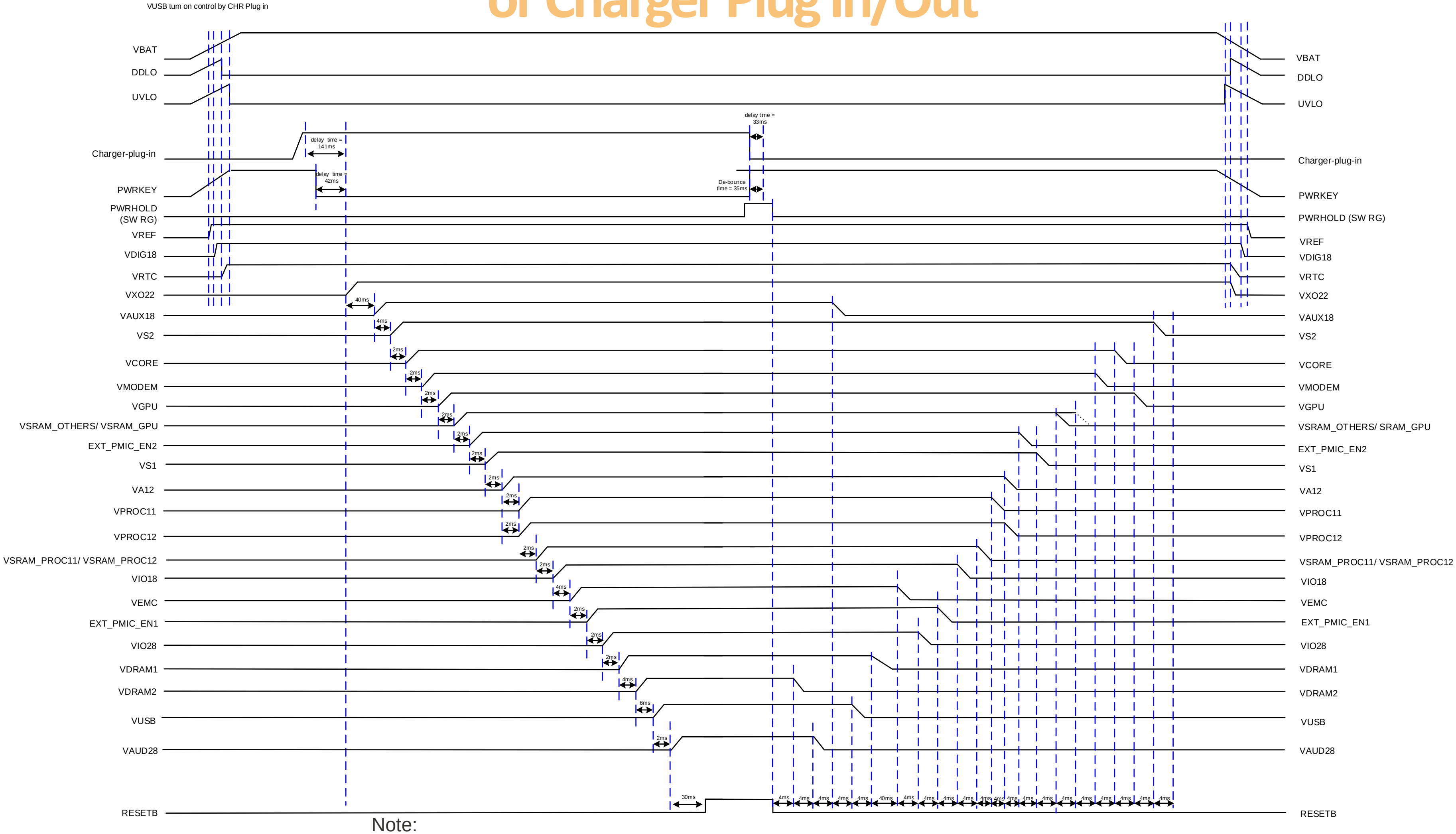
MT6358 w/i ext. Switching Charger



Function Description

Power on/off Sequence by pressing PWRKEY or Charger Plug In/Out



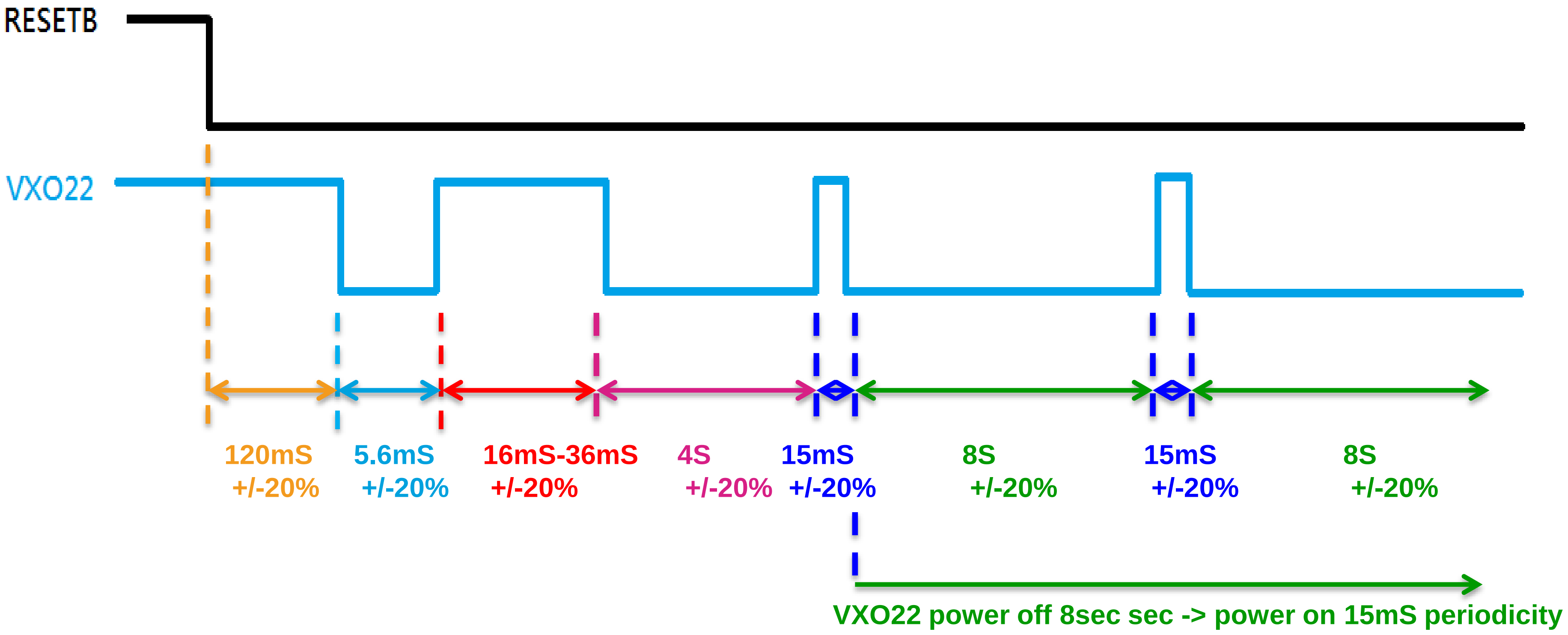
Note:

- Charger-plug in to VXO22 power on De-bounce time spec : +/- 40%
- PWRKEY power on-off timing spec : +/- 20%

RTC EOSC Cali Mode VXO22 Power On/Off Behavior In System Power Off Mode (32K-Less)

- Due to RTC entering to EOSC cali mode in System power off mode. RTC clock source is come from 26MHz (power source is VXO22) in PMIC .

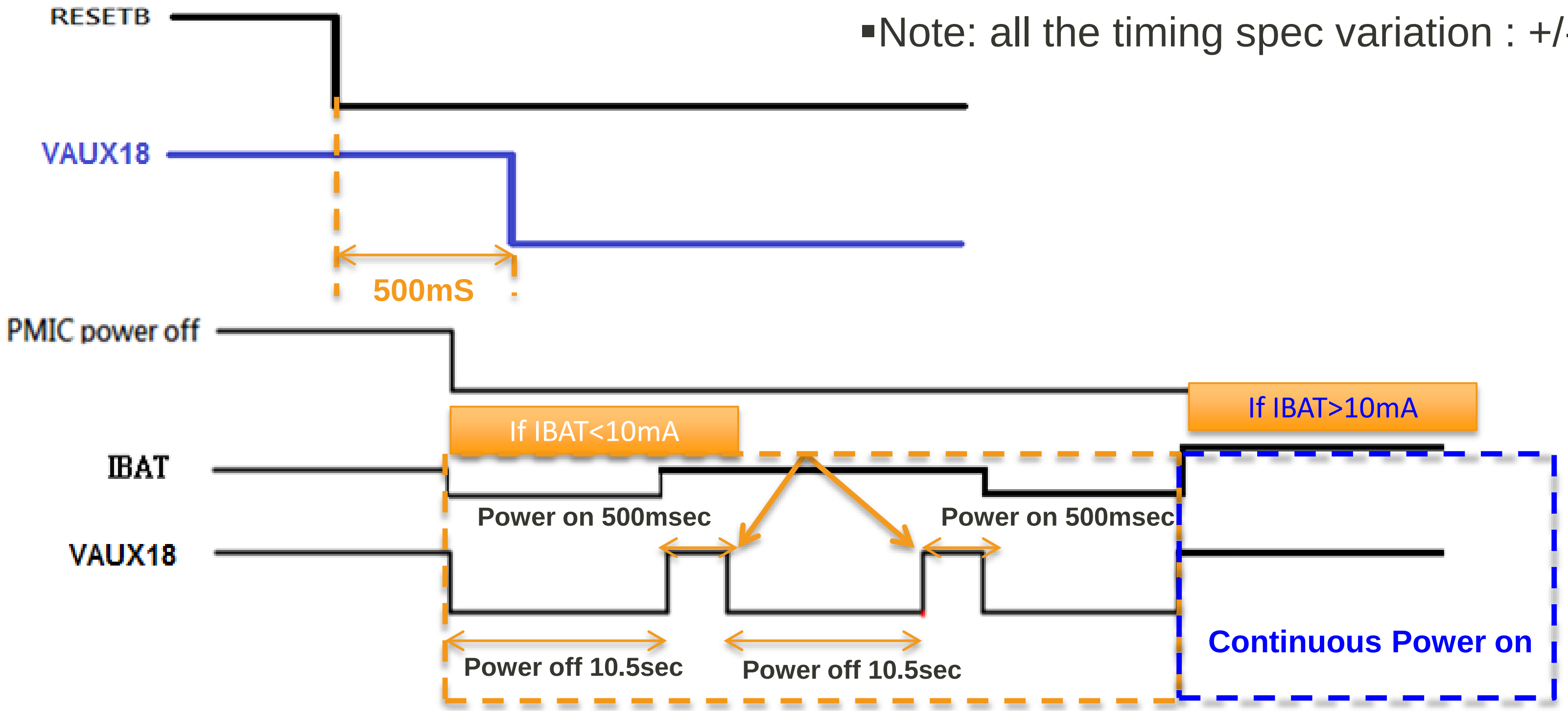
  VXO22 will power on /off periodicity for RTC clock calibration.



VAUX18 Behavior In Power off mode

- GM3.0 Enable , VAUX18 behavior in power off mode
  - ✓ Power off sequence relationship : RESEB low -> 500mS -> VAUX18 low
  - ✓ If IBAT < 10mA
    - VAUX18 turn on 500msec , turn off 10.5sec each cycle to accumulate system power consumption
  - ✓ If IBAT > 10mA
    - VAUX18 continuous power on to accumulate system power consumption.
- GM3.0 disable , VAUX18 follow normal power off sequence.

▪Note: all the timing spec variation : +/-20%



Function Description

UVLO (Under Voltage Lock Out) Spec Summary (1)

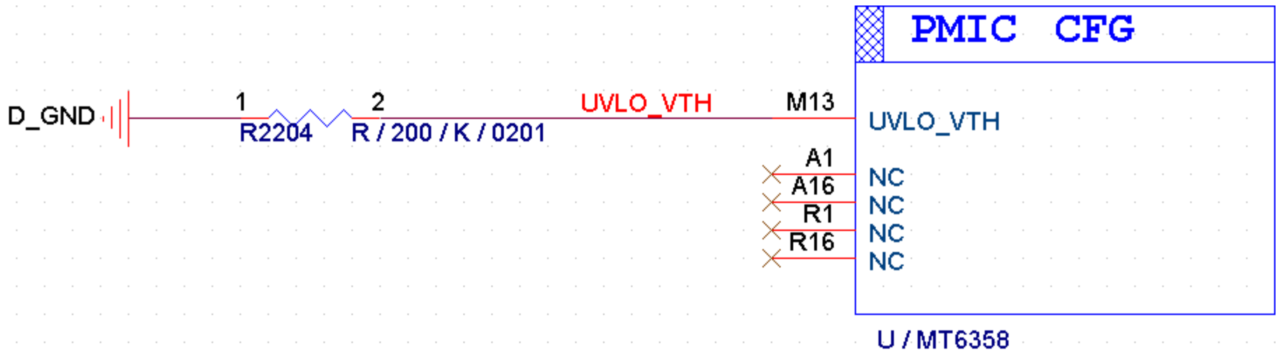
	Condition	MT6358
PIN SEL	UVLO_VTH pin	Yes (1 pin) Select UVLO_VTH by different Resistor
UVLO on	W/O charger in	U1=3.4V~2.9V (0.1V steps) 3.0V(default)
	With Charger in	
UVLO off	UVLO Low threshold	2.9V~2.5V (0.05V steps) 2.6V (default)
Accuracy		± 50mV

Function Description

UVLO (Under Voltage Lock Out) Spec Summary (2)

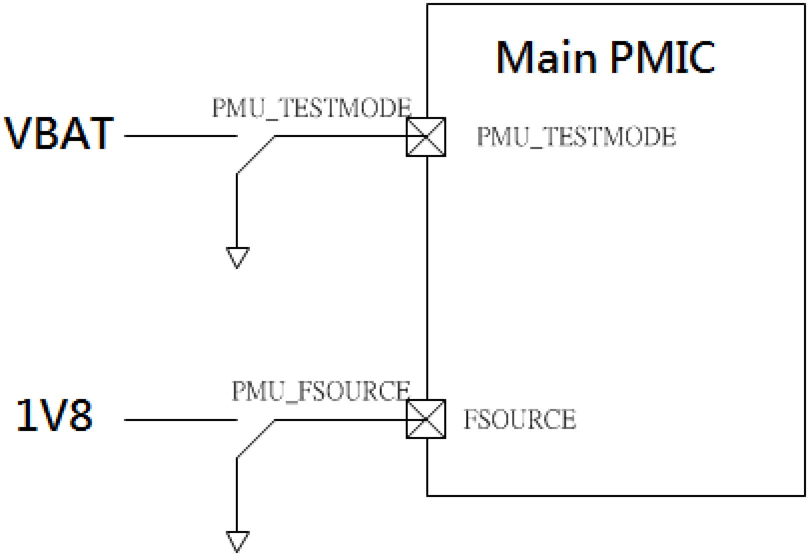
UVLO by Pin selection

- UVLO: 2.9V: <110KΩ
- UVLO: 3.0V: 185KΩ ~ 270KΩ (default 200KΩ)
- UVLO: 3.1V: 460KΩ ~ 560KΩ
- UVLO: 3.2V: 0.925MΩ ~ 1.11MΩ
- UVLO: 3.3V: 1.84MΩ ~ 2.75MΩ
- UVLO: 3.4V: >4.7MΩ



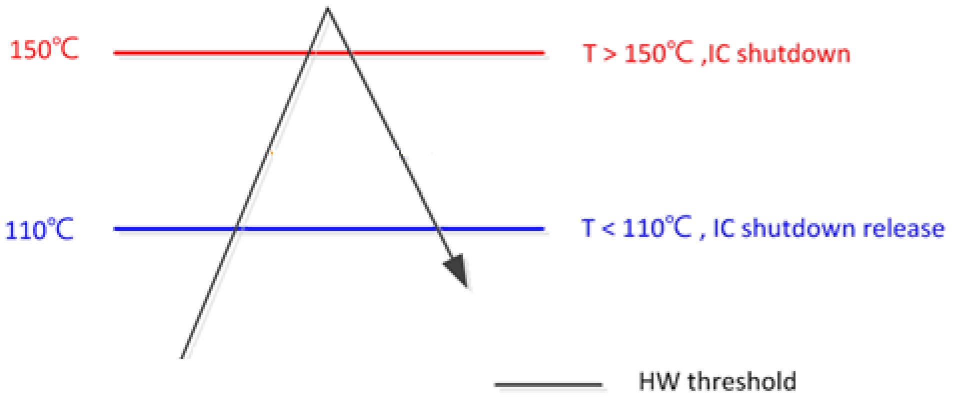
Function Description
PMIC FSOURCE/PMU_TESTMODE

- **FSOURCE/PMU_TESTMODE**
  - These pins should be connected to ground for normal operation.



Application note

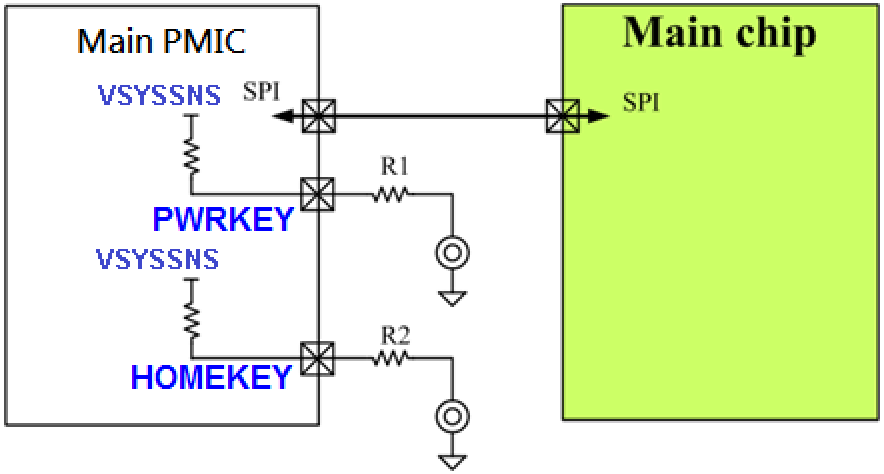
- HW control (+/- 15 ℃)
  - HW shutdown release when Tj < 110 ℃.
  - Tj > 150 ℃ PMU HW shutdown



Function Description

HW External Shutdown Function

HW External Shutdown Function



- **Long press Function of PWRKEY or HOMEKEY**
  - **5 / 8 (default) / 11 / 14 s with < +/-20% accuracy**
    - Timer can be reset by SW (**CLK source =32KHz**)
  - There are 3 option
    - PWRKEY + HOMEKEY (setting by register) **(default)**
    - PWERKEY only (setting by register)
    - HOMEKEY only (setting by register)

Long press Function

- Option 0 : Force PMIC shutdown **(default)**
  - Reset Scope:
    - All default on power turn on by UVLO
    - VRTC28 & VXO22 don't reset in 32Kless mode
- Option 1 : Force PMIC pull RESETB low pulse (8ms) to AP (Smart Reset)

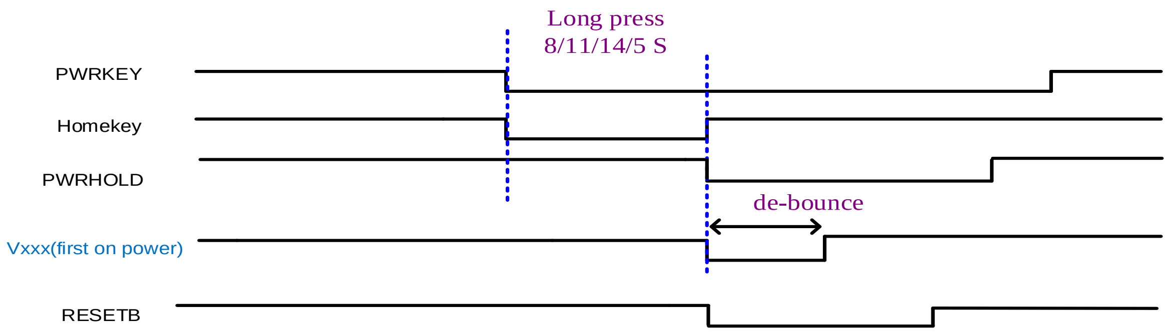
Function Description

Long press shutdown power re-start condition

Re-power on after PMIC shutdown

- There are 3 option
  - Case1: Re-power on if keep long press PWRKEY after PMIC shutdown **(default)**
  - Case2: Re-power on if release PWRKEY after PMIC shutdown
  - Case3: Re-power on if press PWRKEY again after PMIC shutdown

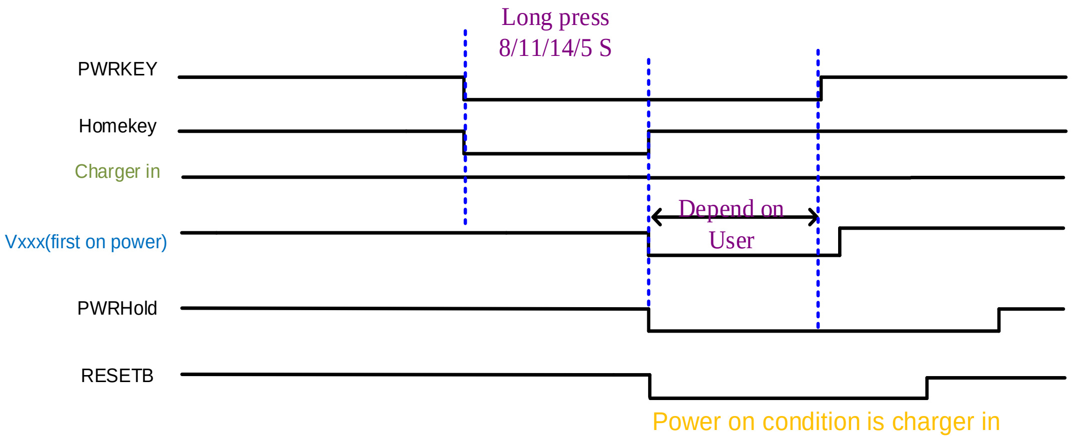
- Case1 : Re-power on if keep long press PWRKEY after PMIC shutdown
  - Re-Power on condition is PWRKEY



Function Description

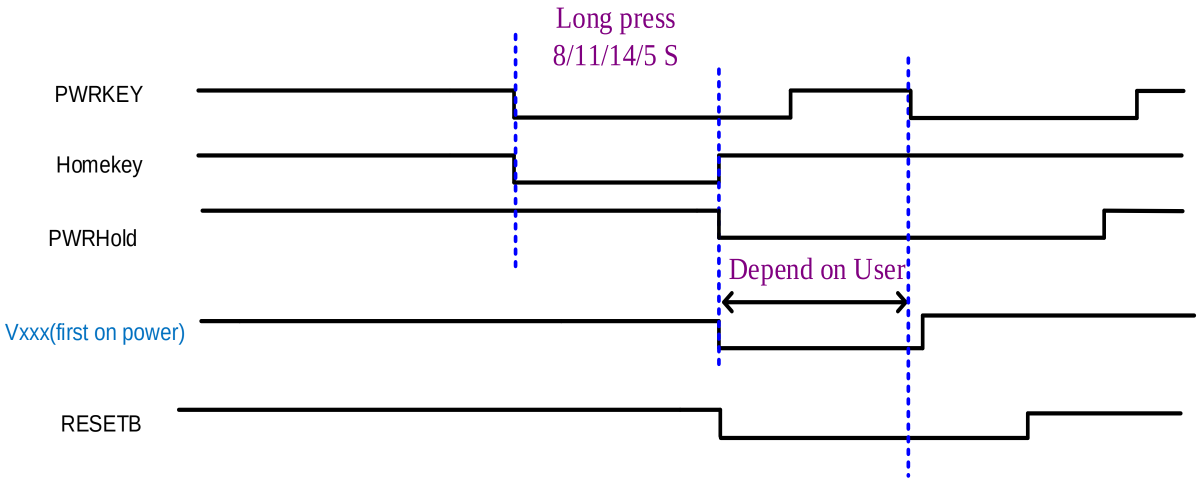
Long press shutdown power re-start condition

- Case2 : Re-power on if release PWRKEY after PMIC shutdown
  - Re-Power on condition is Charger in



Function Description
Long press shutdown power re-start condition

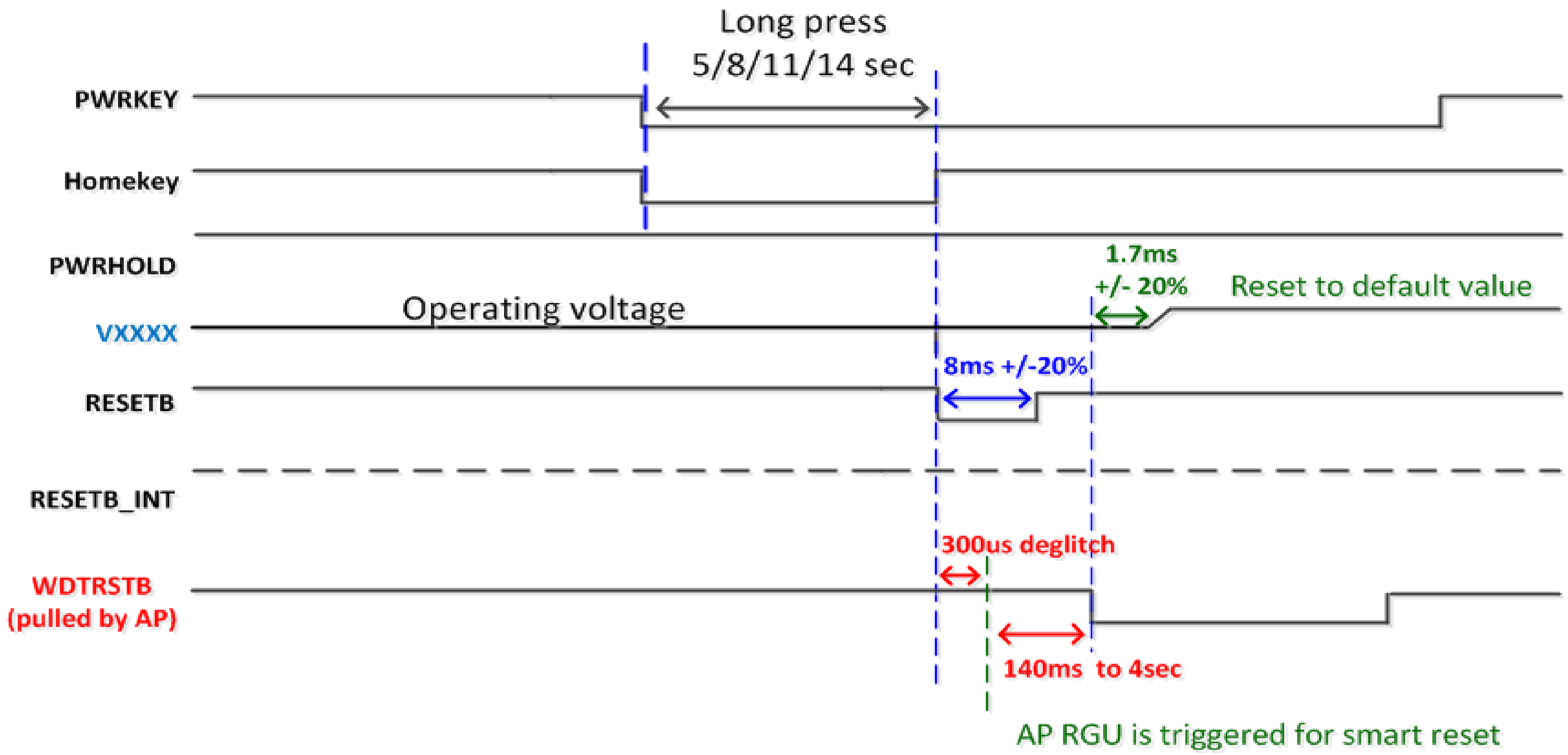
- Case3 : Re-power on if press PWRKEY again after PMIC shutdown
  - Re-Power on condition is PWRKEY



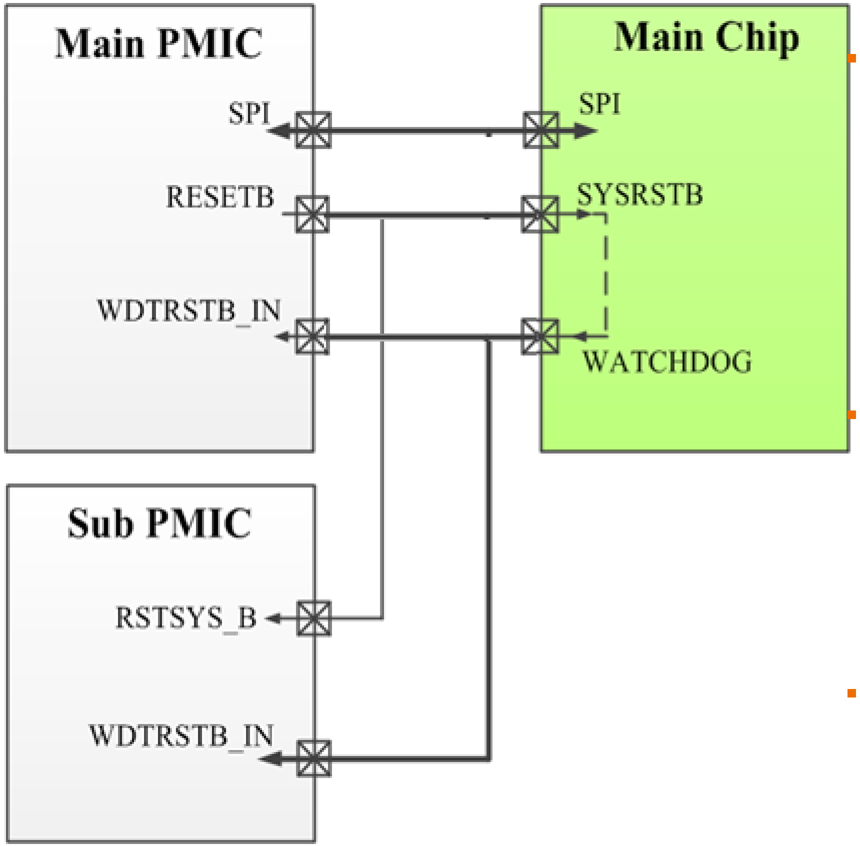
Function Description

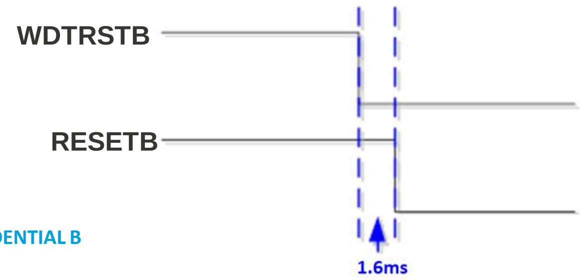
Long press – RESETB reset (Smart Reset)

- Press PWRKEY+HOMEKEY over long press timer to trigger smart reset
  - PMIC only pull RESETB low with a short pulse and then reset by WDTRST
  - need release key and press key again for next RESETB low pulse



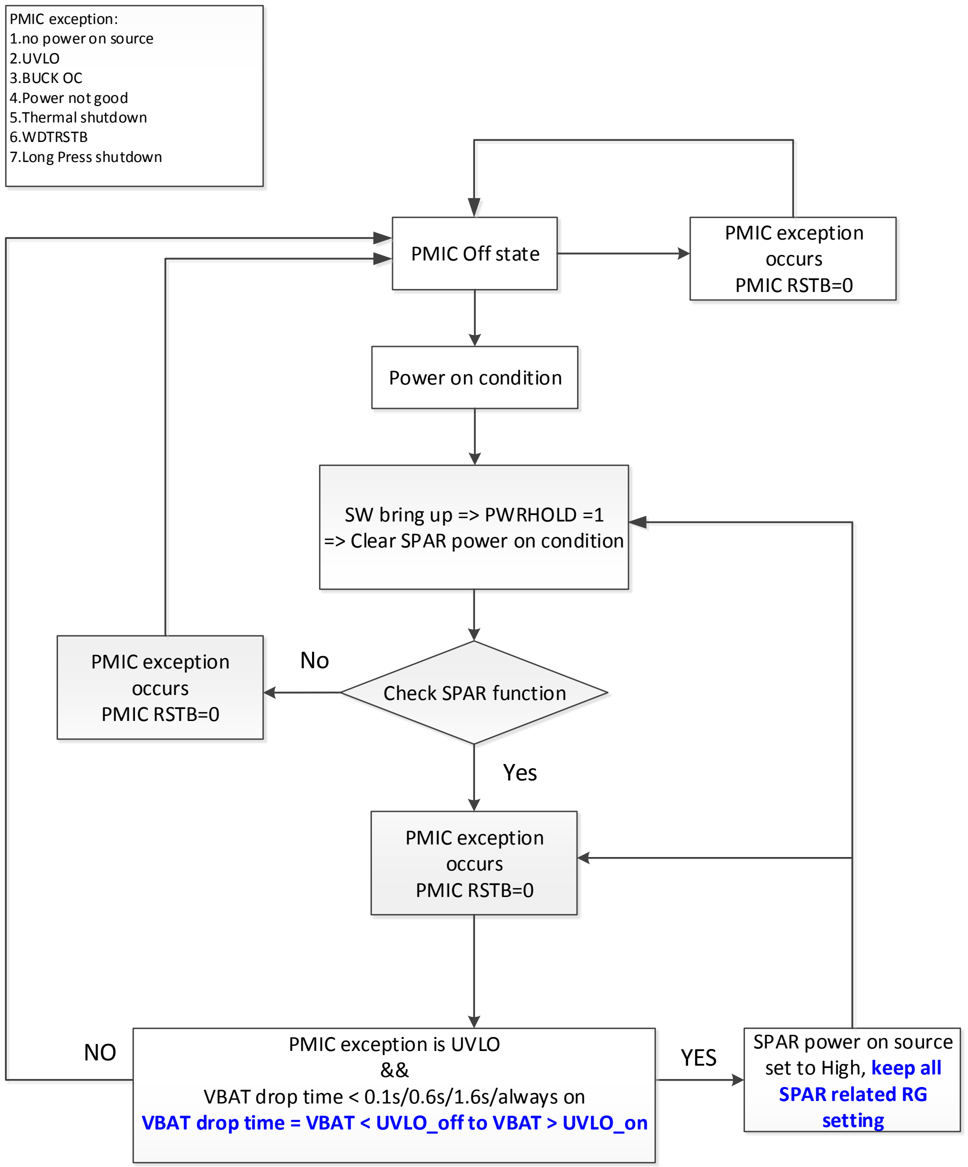
AP Watch Dog timer





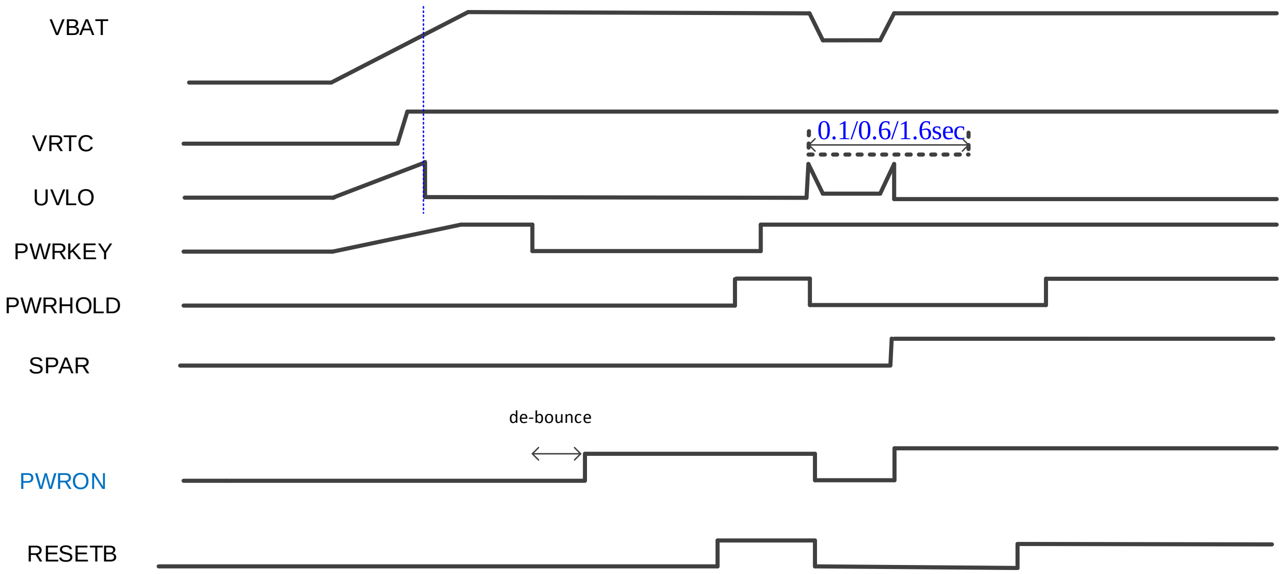
- **SW watchdog reset function (need to enable)**
  - AP **WATCHDOG** should connect to Main PMIC and Sub PMIC **WDTRSTB_IN**
  - AP Watchdog timeout reset send an low signal to **WDTRSTB** (low active) when system hang
  - Main PMIC and Sub PMIC will be reset when **WDTRSTB_IN** PMIC pull down
- **Watchdog reset option**
  - Option 0: Reset PMIC Reg value (default)
  - Option 1: Shutdown PMIC
  - Option 2: Shutdown PMIC then auto re-power-on (Cold Reset)
- **HW PMIC reset function**
  - Add external reset to AP and Main PMIC **SYSRSTB** trace
  - AP will reset when **SYSRSTB** pull down and sent Watchdog signal to Main PMIC and Sub PMIC **WDTRSTB_IN** reset PMIC
  - De-bounce time 1.6ms

SPAR flow chart



SPAR Application note

- Feature support condition
  - VRTC output need coin cell or keep-alive capacitor
- Enabled by software
  - Three time settings can be selected
    - 100ms, VRTC output need coin cell or >2.2uF capacitor
    - 0.6s, VRTC output need coin cell or >4.7uF capacitor
    - 1.6s , VRTC output need coin cell or > 22uF capacitor



Power domain for I/O Pin

Pin Name	Power Source ball name	Power source domain
PWRKEY	VSYSSNS	VSYS
HOMEKEY	VSYSSNS	VSYS
RESETB	DVDD18_IO	VIO18
EXT_PMIC_EN1	VSYSSNS	VSYS
EXT_PMIC_EN2	VSYSSNS	VSYS
WDTRSTB_IN	DVDD18_IO	VIO18
SRCLKEN_IN0	DVDD18_IO	VIO18
SRCLKEN_IN1	DVDD18_IO	VIO18
SPI_CSN	DVDD18_IO	VIO18
SPI_CLK	DVDD18_IO	VIO18
SPI_MOSI	DVDD18_IO	VIO18
SPI_MISO	DVDD18_IO	VIO18

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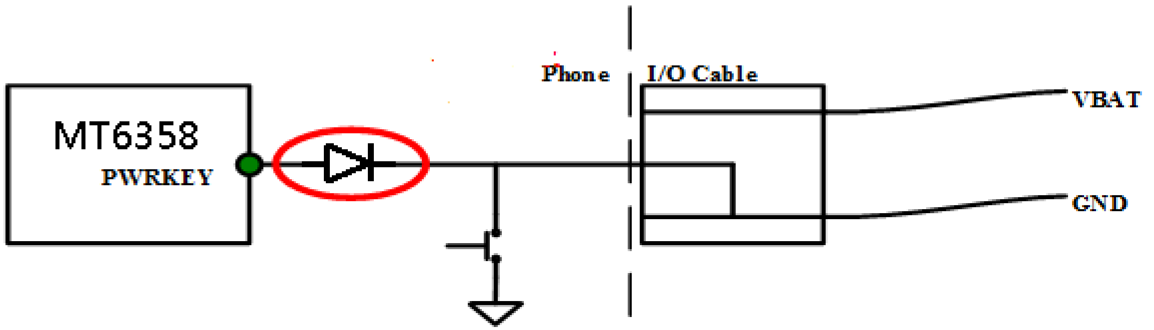
Reference Design

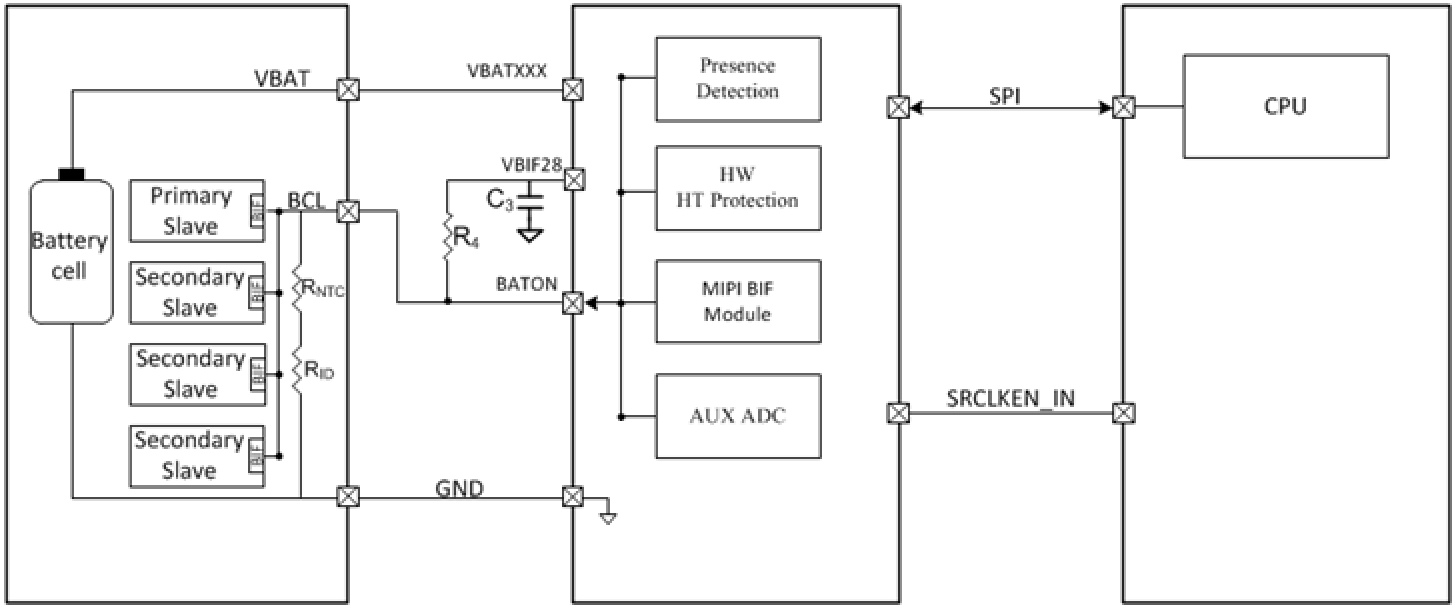
IC Protection: PWRKEY



Please reserve schottky diode(VF<0.3V@1mA) on phone PCB to protect **PWRKEY** no matter if PWRKEY connect to any I/O connector or not.

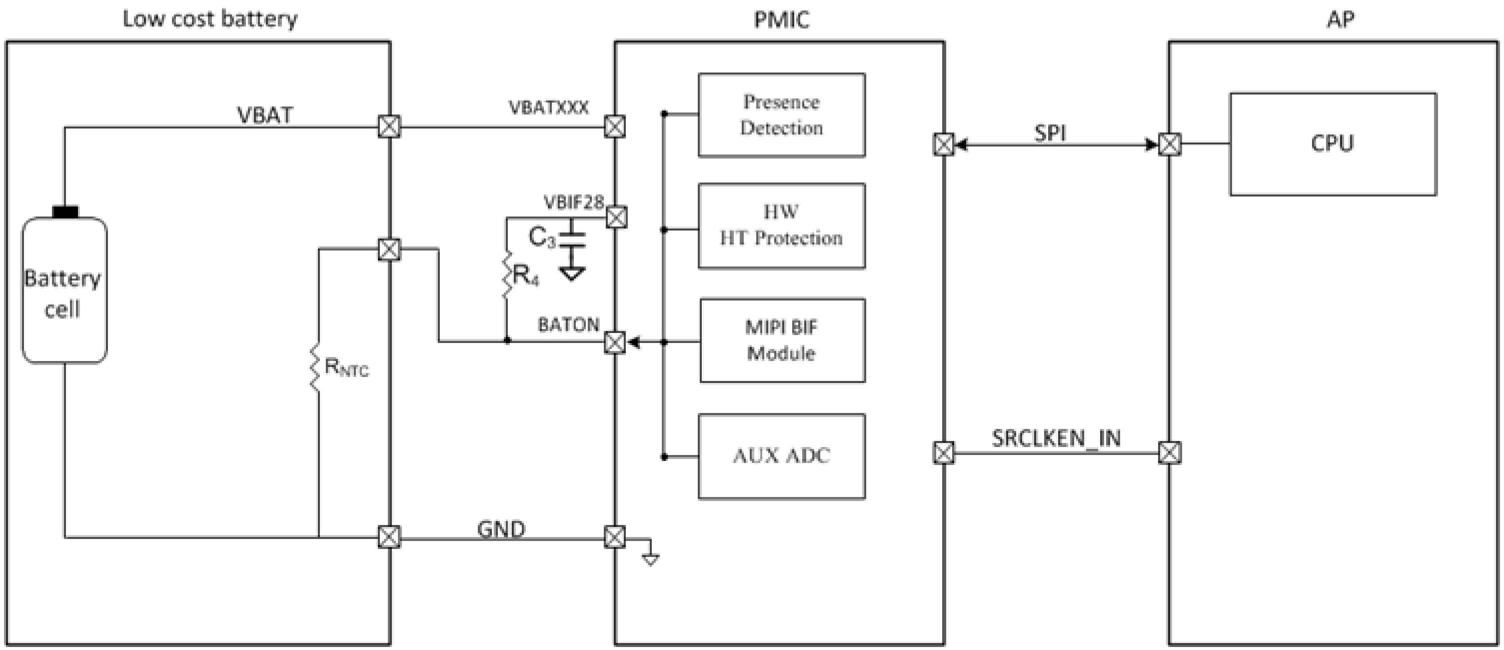
BAT_ON

Block Diagram for Smart battery
3-PIN Smart Battery



- *KEY FEATURES*
  - MIPI BIF Smart Battery Supported - Single-master/ Multi-slave
  - HW Battery Pack Presence/ Removal Detection
  - Charger HW HT Thermal Protection
  - Temperature Monitoring by AUXADC

Block Diagram for Low cost battery



- *KEY FEATURES*
  - HW Battery Pack Presence/ Removal Detection
  - HW HT Thermal Protection
  - Temperature Monitoring by AUXADC
  - Low Cost Battery Supported

HW Battery Presence Detection

- Battery presence is detected by sensing the existence of R_{NTC} resistor inside the battery pack.
- Dedicated comparator is used for Battery Pack Presence/ Removal Detection.
  - Battery pack is considered not present if BAT_ON is above **0.964*VBIF**.
  - Interrupts are generated when detecting battery insertion or removal
  - Charging shall be stopped upon battery removal

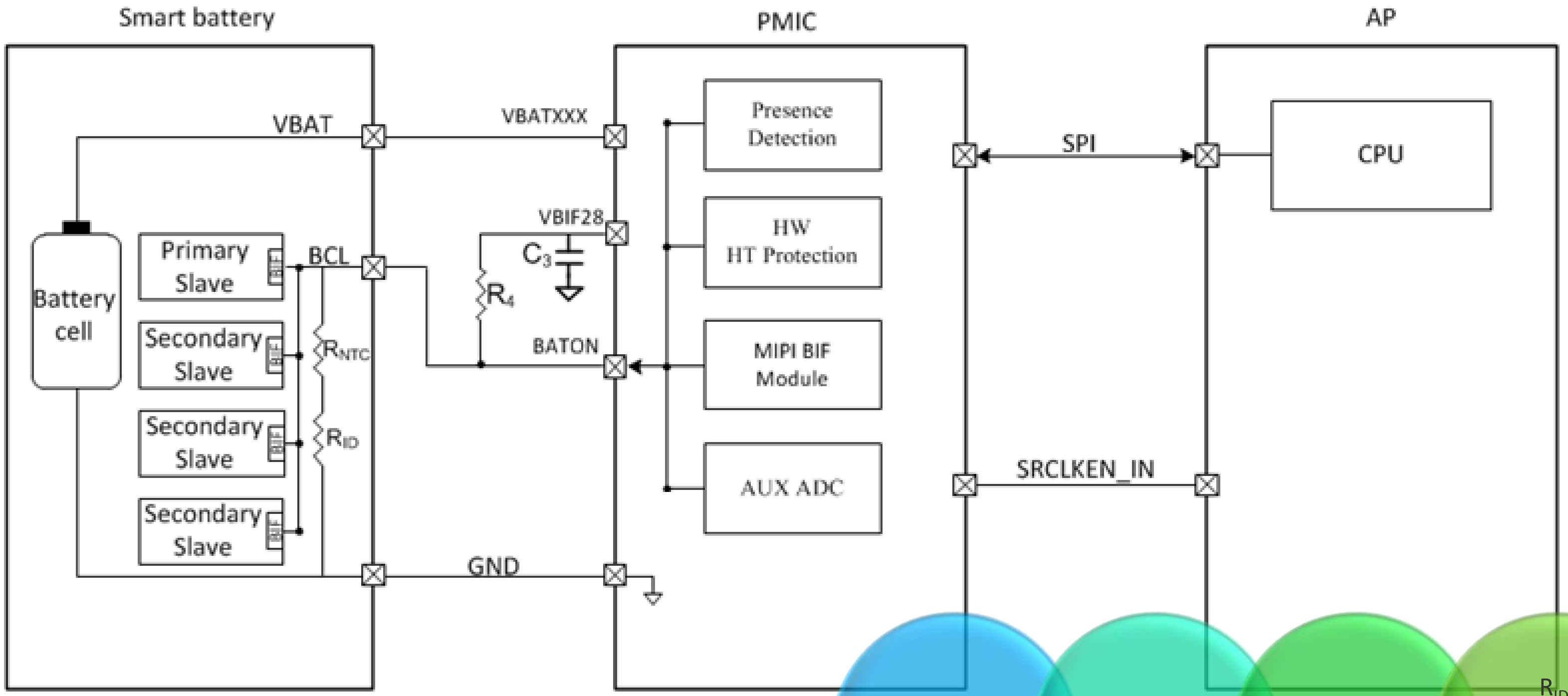
Parameter	Min	Typ	Max	Units
Presence Detection comparator threshold	(0.964*VBIF)-20mV	0.964*VBIF	(0.964*VBIF)+20mV	V

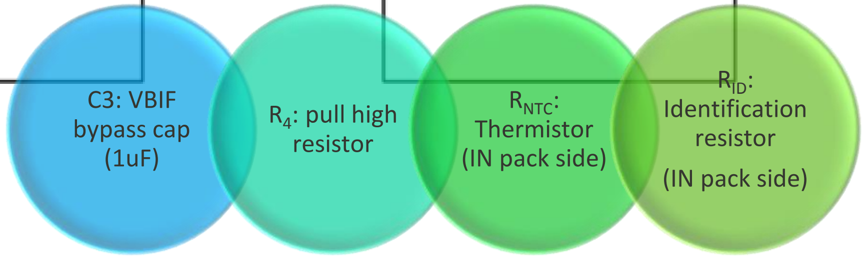
Battery High Temperature Protection

- Dedicated comparator are used to detect battery overheat.
  - Six configurable thresholds selected by register setting.
  - Battery stops charging if BATON voltage is below HT thermal protection thresholds.

Parameter	Min	Typ	Max	Units	Temperature Typ.
Battery HT thermal protection for low cost battery	263	273	283	mV	65 degC
	303	313	323	mV	60 degC
	350	360	370	mV	55 degC
Battery HT thermal protection for 3-PIN smart battery	1212	1222	1232	mV	65 degC
	1228	1238	1248	mV	60 degC
	1246	1256	1266	mV	55 degC

Schematics/layout notice





- VBIF need bypass cap 1uF
- BATON trace total capacitance :
  - should be smaller than 50pf with Smart battery
  - should be smaller than 500pf with Low cost battery

Battery Pack NTC Selection Criteria

- Note 1: Battery pack NTC selection criteria
  - R_{NTC}: 10k±1% at 25 ℃, and β-constant(25 ℃-50 ℃)(K)=3380K ±3% or ±1%
  - R_{NTC}: 47k±1% at 25 ℃, and β-constant(25 ℃-50 ℃)(K)=4050K ±3% or ±1%

NTC spec example :

Part Number	Resistance (25°C)	B-Constant (25-50°C) (K)	Max. Operating Current (25°C) (mA)	Rated Electric Power (25°C) (mW)	Typical Dissipation Constant (25°C) (mW/°C)	Operating Temperature Range (°C)
NCP18XQ102□03RB	1.0k ohm	3650 ±3%	1.00	100	1	-40 to 125
NCP18XW152□03RB	1.5k ohm	3950 ±3%	0.81	100	1	-40 to 125
NCP18XW222□03RB	2.2k ohm	3950 ±3%	0.67	100	1	-40 to 125
NCP18XW332□03RB	3.3k ohm	3950 ±3%	0.55	100	1	-40 to 125
NCP18XM472□03RB	4.7k ohm	3500 ±3%	0.46	100	1	-40 to 125
NCP18XW682□03RB	6.8k ohm	3950 ±3%	0.38	100	1	-40 to 125
NCP18XH103□03RB	10k ohm	3380 ±3%	0.31	100	1	-40 to 125
NCP18XW153□03RB	15k ohm	3950 ±3%	0.25	100	1	-40 to 125
NCP18XW223□03RB	22k ohm	3950 ±3%	0.21	100	1	-40 to 125
NCP18WB333□03RB	33k ohm	4050 ±3%	0.17	100	1	-40 to 125
NCP18WB473□03RB	47k ohm	4050 ±3%	0.14	100	1	-40 to 125
NCP18WD683□03RB	68k ohm	4150 ±3%	0.12	100	1	-40 to 125
NCP18WF104□03RB	100k ohm	4250 ±3%	0.10	100	1	-40 to 125
NCP18WM154□03RB	150k ohm	4500 ±3%	0.08	100	1	-40 to 125
NCP18WM224□03RB	220k ohm	4500 ±3%	0.06	100	1	-40 to 125
NCP18WM474□03RB	470k ohm	4500 ±3%	0.04	100	1	-40 to 125

Both flow and reflow soldering methods can be employed.
A blank column is filled with resistance tolerance codes. (J: ±5%, K: ±10%)
Tolerance ±1% NCP18XH103F03RB is also availalbe for 10k ohm type.

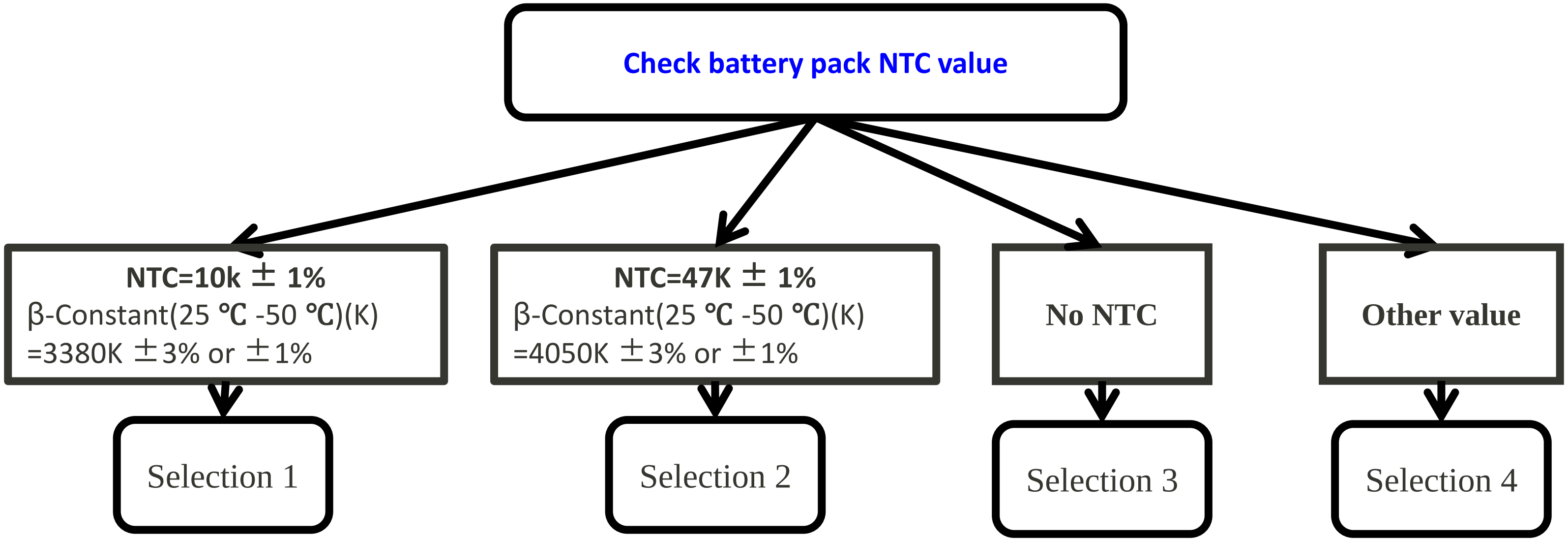
Battery Pack NTC Selection Criteria

Battery Temperature Measure Accuracy

- Battery temperature measure accuracy depend on NTC accuracy and β-constant (25 ℃-50 ℃)(K) accuracy selection

NTC Accuracy @ 25℃	**1%**	**1%**	**5%**
β-constant (25℃-50℃)(K) Accuracy	1%	3%	3%
Battery temperature measure accuracy spec	< ±3℃	< ±4℃~±5℃	< ±6℃~±7℃

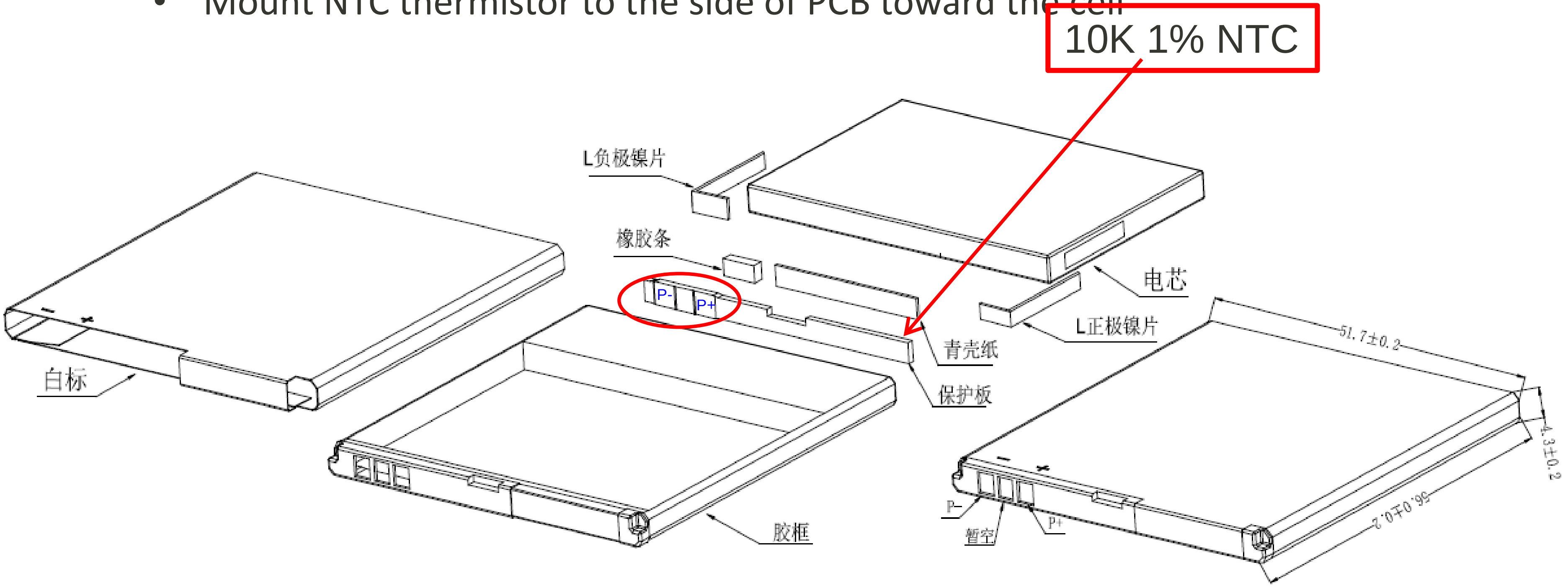
R4 Selection Guide



	Battery type	R4 selection
Selection 1	Low cost battery	R4 select 24K ±1%
Selection 2	Low cost battery	R4 select 90K ±1%
Selection 3	Low cost battery	R4 NC and BAT_ON pin 10K 1% to GND (Without battery temperature information, thermal protection, and battery presence detection.)
Selection 4	Low cost battery	R4 select [$(R_{NTC@-10°C}/8)$ ~ $(R_{NTC@60°C}*8)$] ±1%

Note 1: Recommended Location of NTC in Battery Pack

- **Recommended location of NTC in battery pack**
  - Move NTC thermistor away from P+ and P-
  - Mount NTC thermistor to the side of PCB toward the cell



Note 2: Confirm to meet the above specifications

- Violation of the above specifications will result in measurement error of battery's temperature.

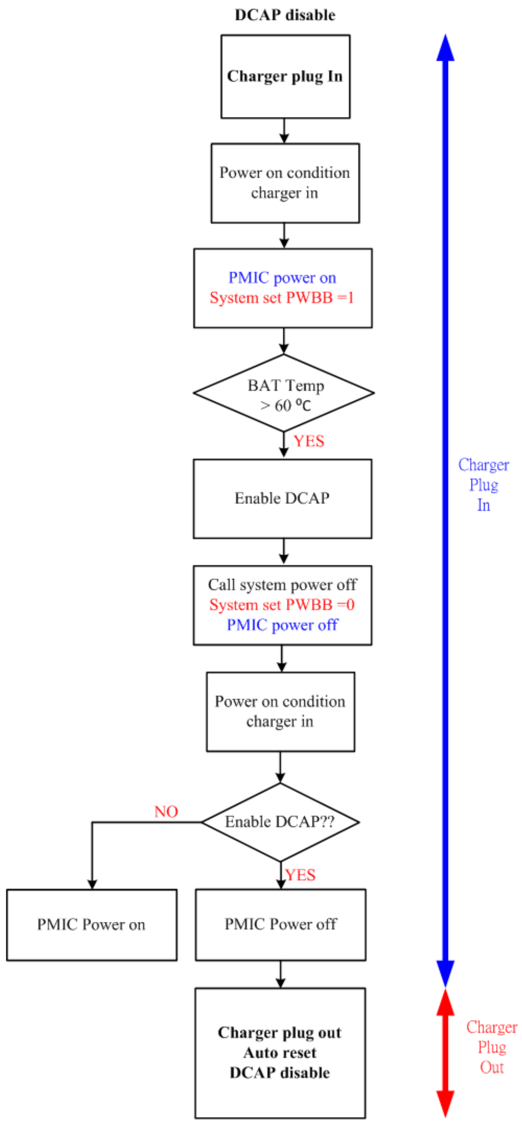
Battery will be under dangerous environment.

Appendix

Safety Protect function when High Temperature

- Disable charger in auto power on (DCAP) condition when high temperature
  - Enable flow
    - Set DCAP enable by SW when charger in and BAT temp > HT shutdown level (default 60°C)
  - Release flow
    - DCAP disable is auto reset when charger plug out

※ DCAP enable flow need follow programming guide setting



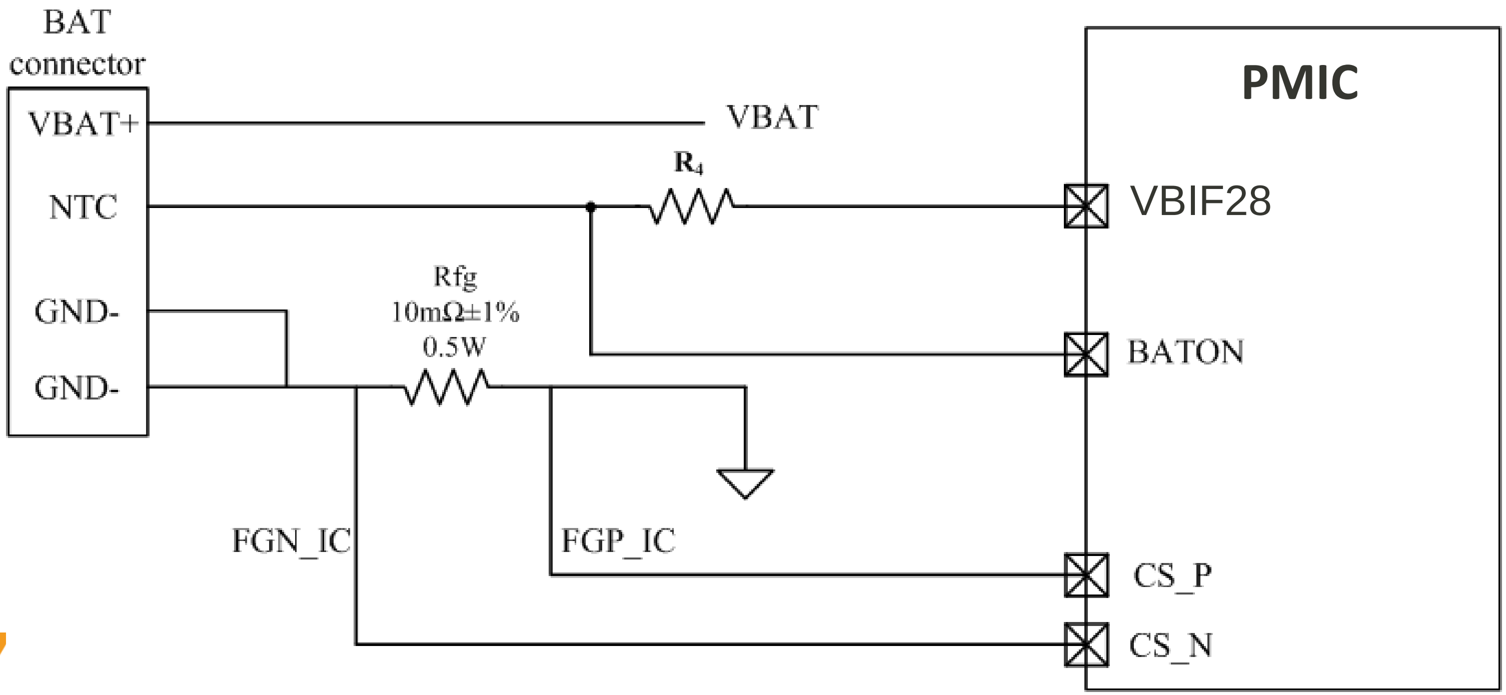
Content

- MT6358 Introduction
- Function Description
- Reference Design
- **Function Block Notice**
- PCB Layout Guideline

Fuel Gauge

Fuel gauge Schematics/layout notice

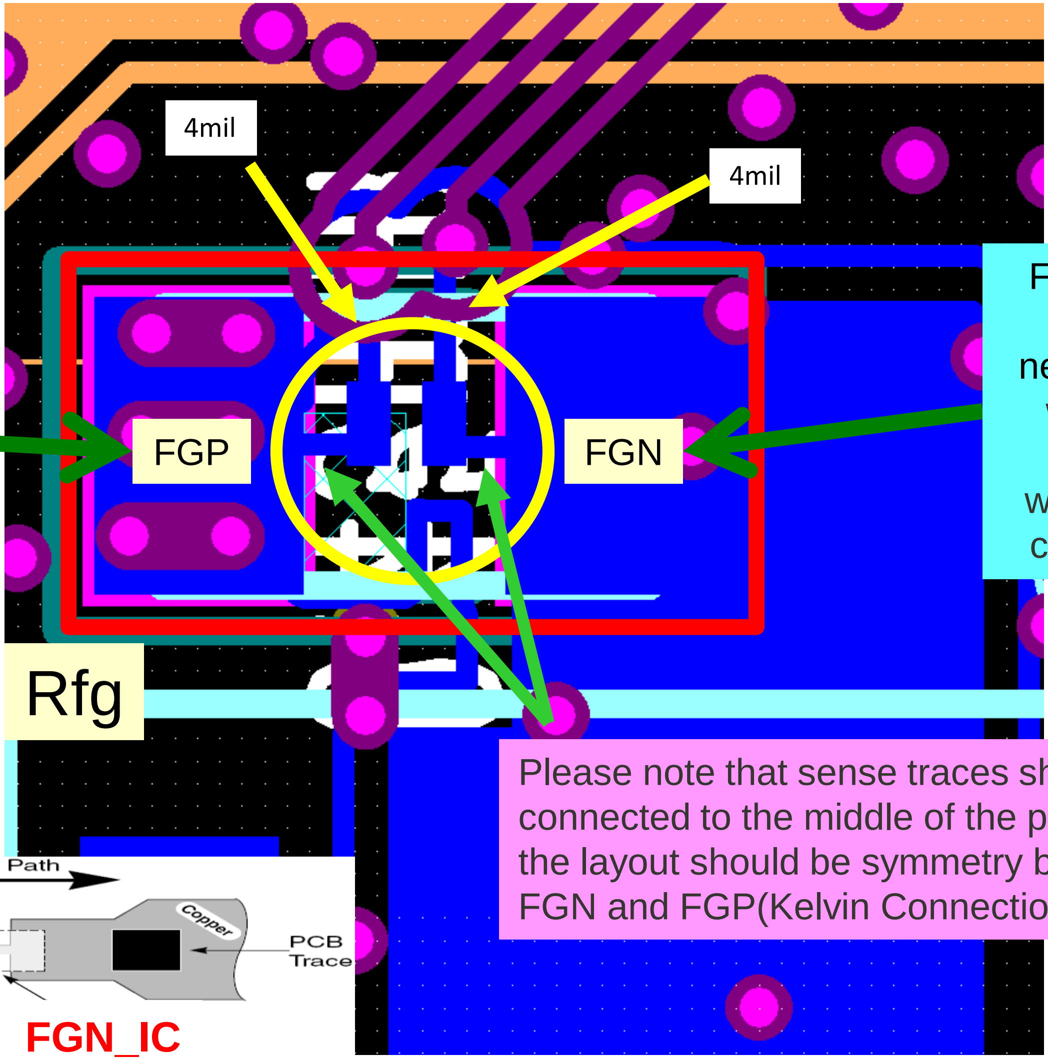
- 1 : Sense resistor Rfg should be **10m Ω 1% ,0.5W↑(depend on system max power consumption 7A-> 0.5W, 10A -> 1W) package** in series with battery negative terminal to ground
  - **System max power consumption < 10A, Rfg is 10mΩ**
  - **System max power consumption > 10A, Rfg is 5mΩ**
- 2： Rfg should be placed near battery connector in PCB layout.
- 3： FGP_IC/FGN_IC should be 4mil **differential traces** from chip CS_N/CS_P to Rfg



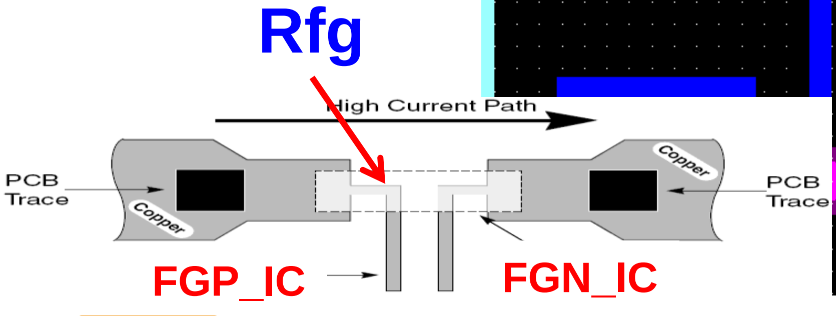
FGN_IC/FGP_IC Layout Example

FGP is connected to system GND. It needs adequate amount of VIAs to system GND in order to withstand system current consumption.

FGN is connected to BATTERY GND. It needs adequate trace width to BATTERY GND In order to withstand the system current consumption



Please note that sense traces should be connected to the middle of the pads and the layout should be symmetry between FGN and FGP(Kelvin Connection).



GM3.0 Board Offset Calibration Test point (Option)

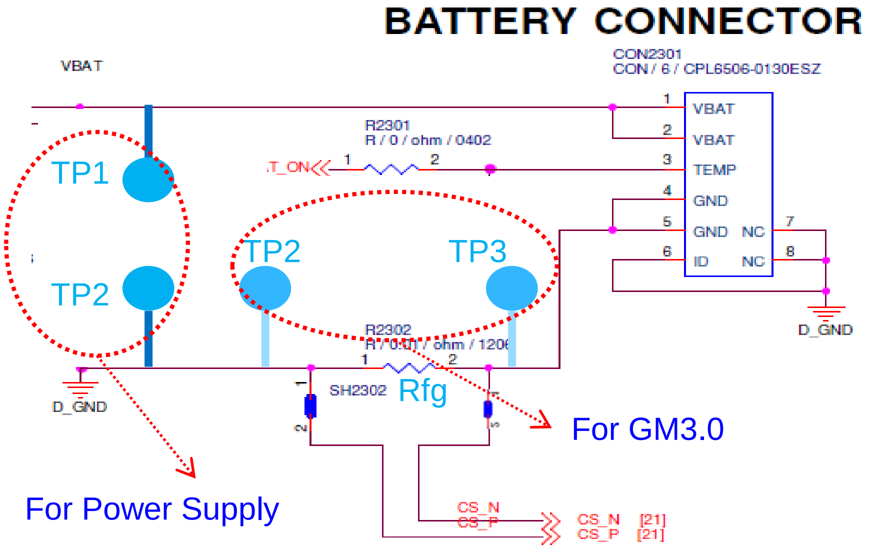
✓TP1 & TP2 for system power supply

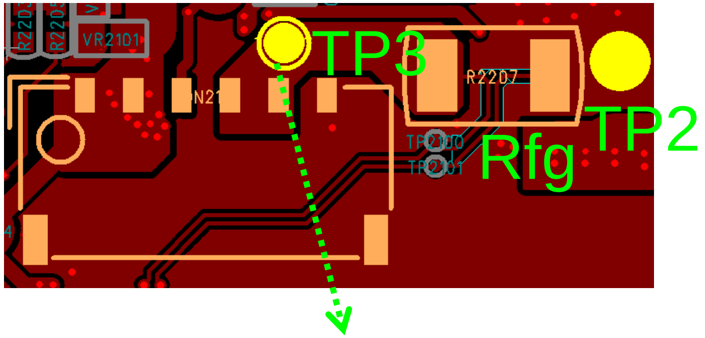
——The test point should on the main trace， as it is used for power input point

✓TP2 & TP3 for GM3.0 calibration

——The test point should on the main trace， or the width of trace to test point should not less than 40 mil as the current would be 1000mA

——The test point DO NOT draw from the trace of CS_N &CS_P

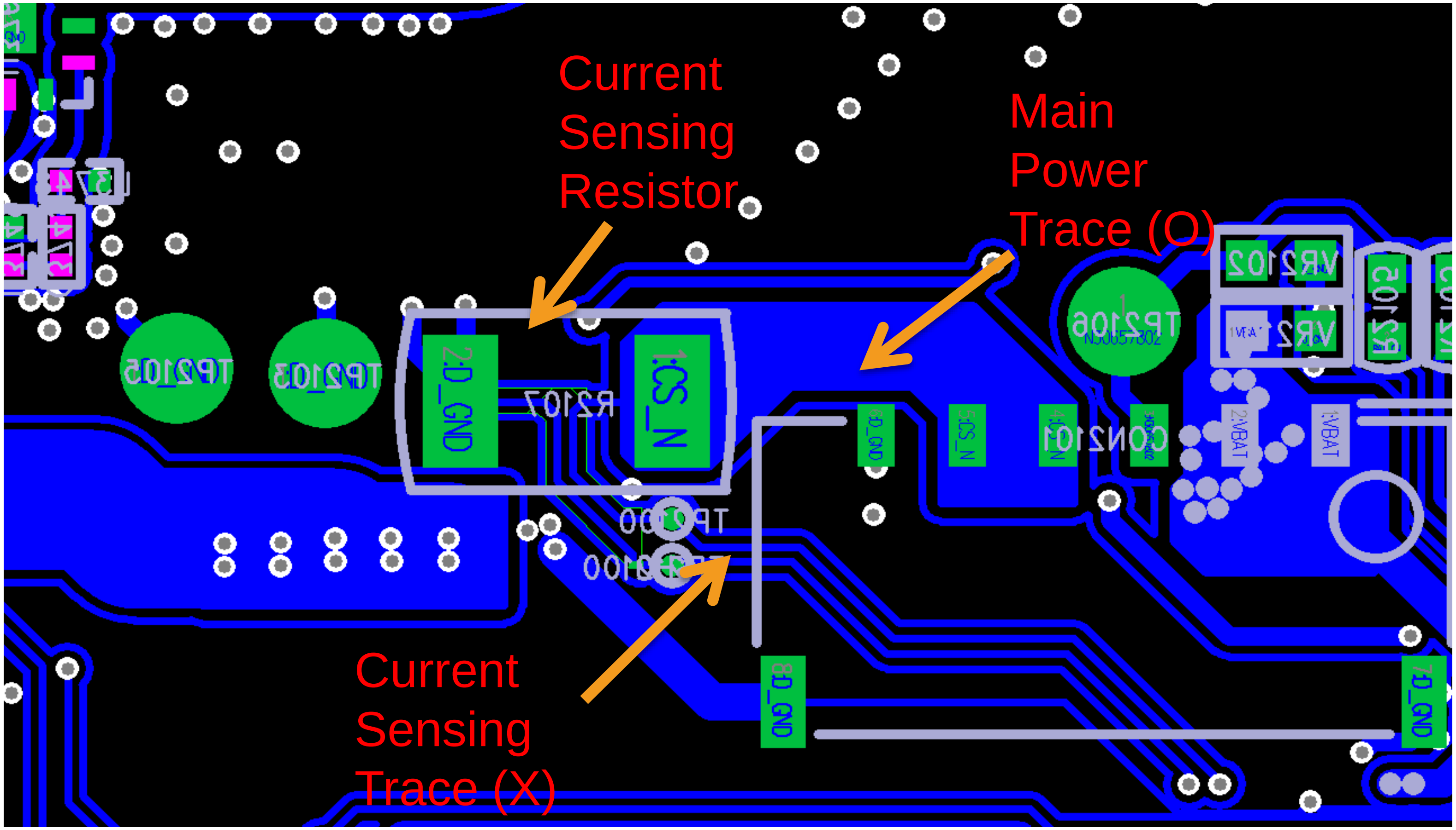




The TP3 is on the trace between CS_N Pad to Battery GND

Layout Example

- TP should be placed on main power trace, not on current sensing trace.

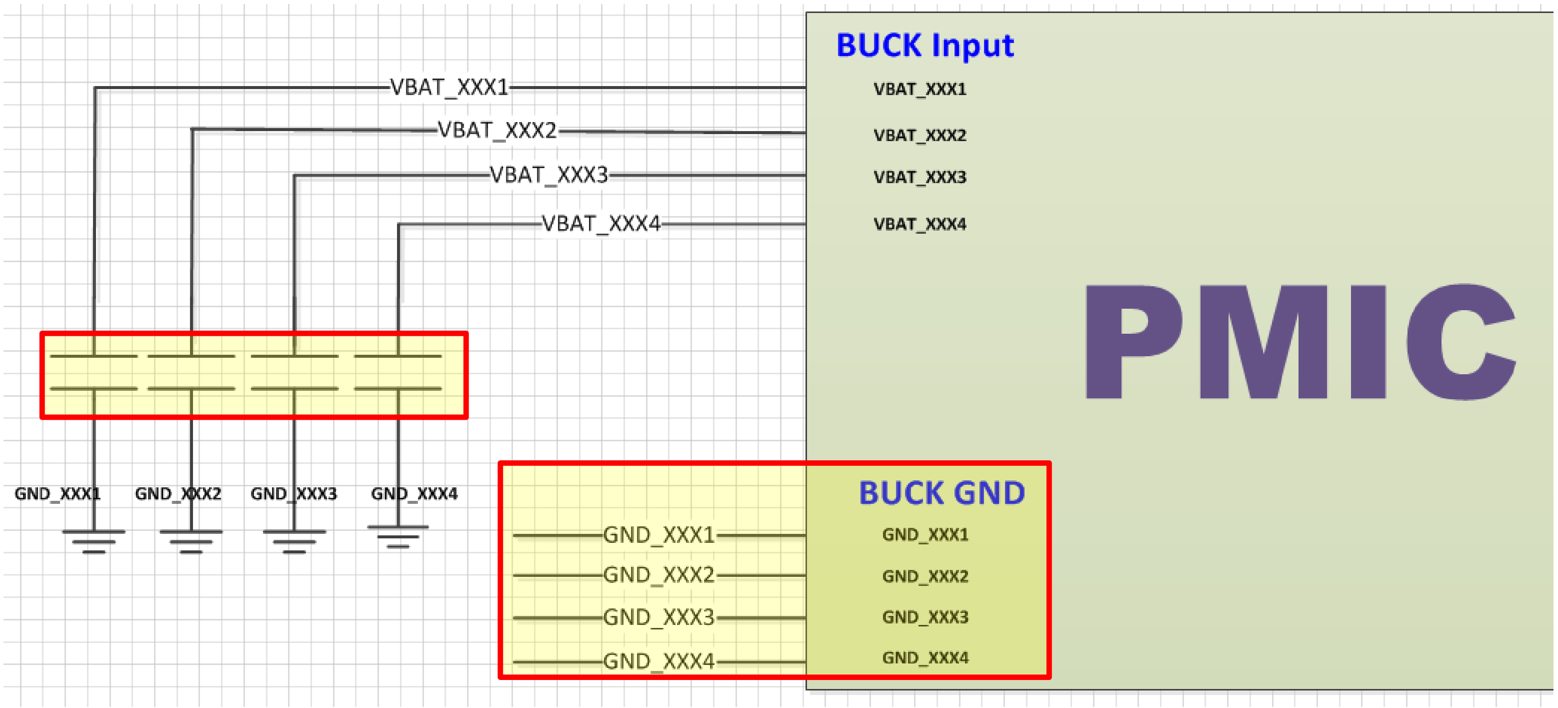


DC-DC

Schematic/Layout Notice

Input decoupling placement and GND layout guide

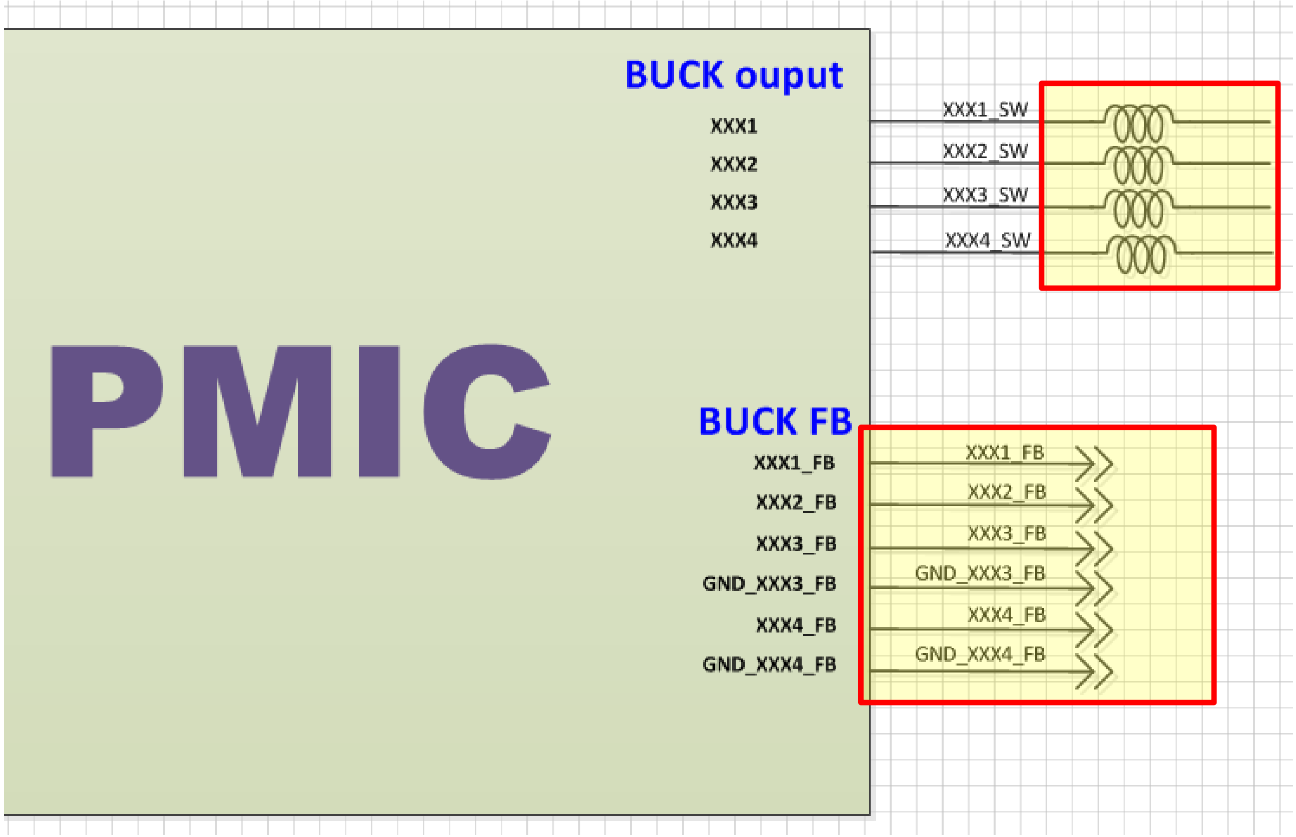
- Please place CIN as close to PMIC as possible and put in shield case.
- GND_VBUCKs x balls(as highlight in following fig.) must connect to related input cap first, and then connect to main GND plane.



Schematic/Layout Notice

Output decoupling placement and schematic guide

- Place power inductors as closer to PMIC balls as possible and put in shield case.
- VBUCK_FB & GND_VBUCK_FB layout should follow PCB layout constraint.



Schematic/Layout Notice

Buck Converter List and Input/Output Decoupling

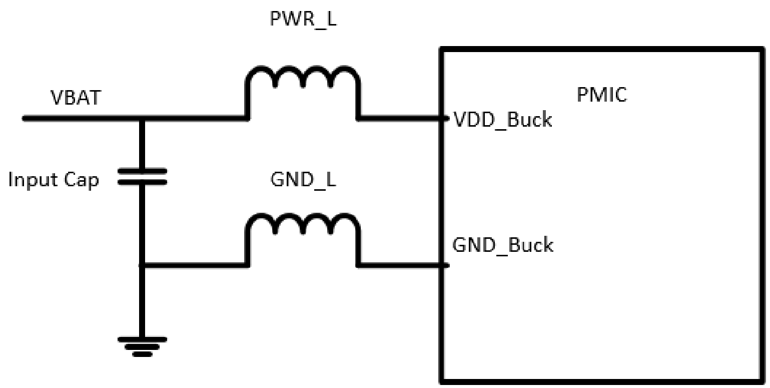
Regulator	Output Current(mA)	Input Decoupling (Rating ≥ 6.3V)	Input Decoupling (Rating ≥ 10V)	Output Decoupling (min)
VS1	2000	≥4.7uF	≥2.2uF	22uF*2+4.7uF (Rating ≥ 6.3V)
VS2	2000	≥4.7uF	≥2.2uF	22uF (Rating ≥ 6.3V)
VDRAM1	2000	≥4.7uF	≥2.2uF	LPDDR4x : 22uF*3 (Rating ≥ 6.3V) LPDDR3 : 22uF*2 (Rating ≥ 6.3V)
VMODEM	3250	≥4.7uF	≥2.2uF	22uF*2 (Rating ≥ 6.3V)
VPA	1000	≥10uF	≥4.7uF	1uF+6.2uF (Rating ≥ 10V)
VPROC11	4600	≥10uF	≥4.7uF	22uF*2 (Rating ≥ 6.3V)
VPROC12	3190	≥10uF	≥4.7uF	22uF*2 (Rating ≥ 6.3V)
VCORE	4600	≥10uF	≥4.7uF	22uF*2 (Rating ≥ 6.3V)
VGPU	3310	≥10uF	≥4.7uF	22uF*2 (Rating ≥ 6.3V)

Note: *1 for VPA out cap distribution, please refer “VPA Output Capacitance Notice”

Schematic/Layout Notice

BUCK input cap to IC ball layout inductor value constraint

- MMD spec => the spec of trace parasitic inductance from buck input cap to PMIC Ball
- PWR_L+GND_L < Spec



Schematic/Layout Notice

BUCK input cap to IC ball layout inductor value constraint

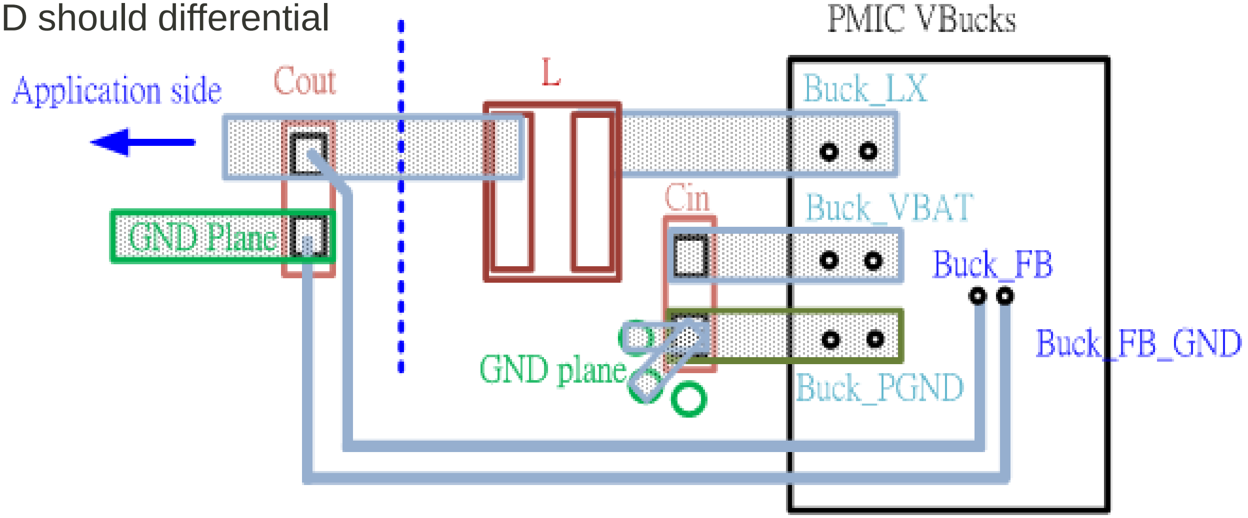
DCDC	Input Trace (from Caps/ Inductor to IC ball)	MT6358 SPEC for Inductance
VS1	VSYS_VS1	L_power + L_Ground < 2nH
	GND_VS1	
VS2	VSYS_VS2	L_power + L_Ground < 2nH
	GND_VS2	
VDRAM1	VSYS_VDRAM1	L_power + L_Ground < 2nH
	GND_VDRAM1	
VPA	VSYS_VPA	L_power + L_Ground < 1.5nH
	GND_VPA	
VMODEM	VSYS_VMODEM	L_power + L_Ground < 2nH
	GND_VMODEM	
VPROC11	VSYS_VPROC11	L_power + L_Ground < 1nH
	GND_VPROC11	
VPROC12	VSYS_VPROC12	L_power + L_Ground < 1nH
	GND_VPROC12	
VCORE	VSYS_VCORE	L_power + L_Ground < 1nH
	GND_VCORE	
VGPU	VSYS_VGPU	L_power + L_Ground < 1nH
	GND_VGPU	

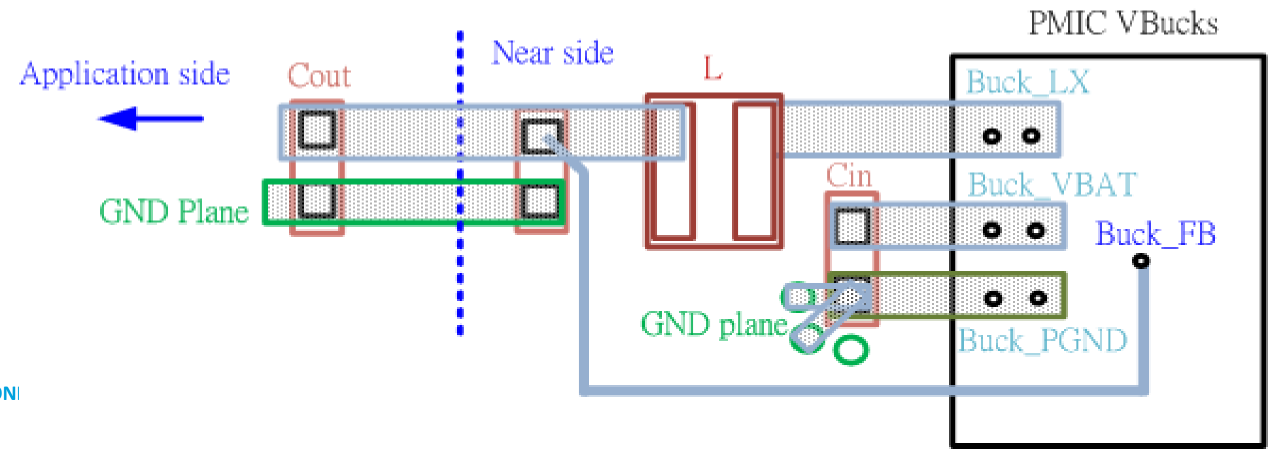
Schematic/Layout Notice

layout guide

- Inductance need to follow application notice that has components selection guide.
- Placement, layout and schematic need to follow checklist.

FB/FB_GND should differential

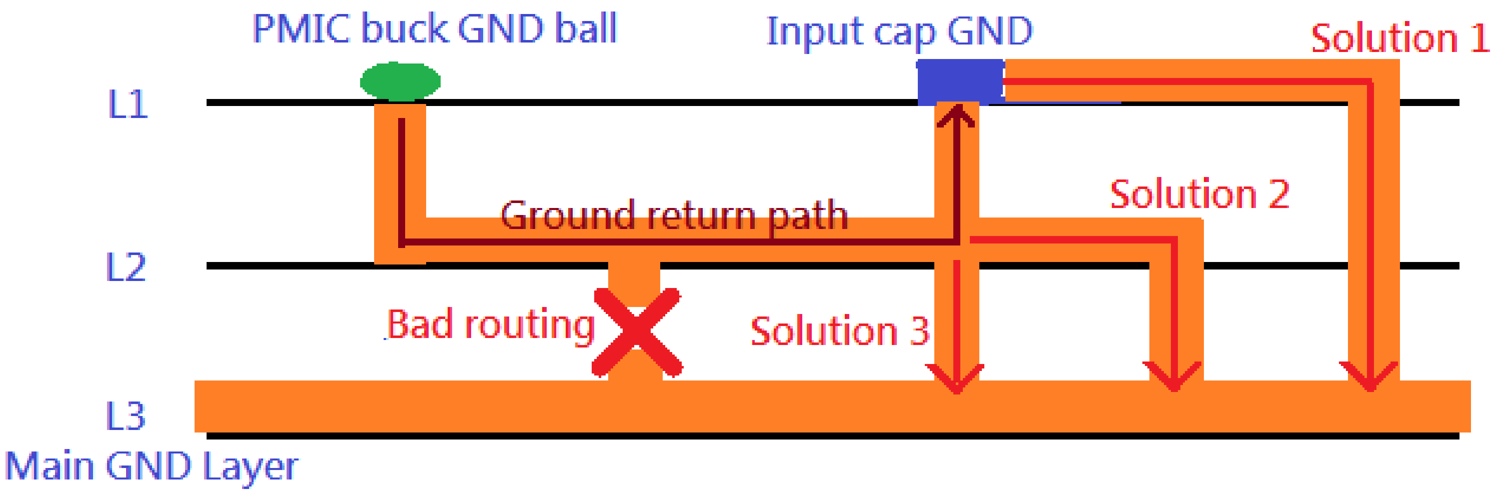




Schematic/Layout Notice

layout guide

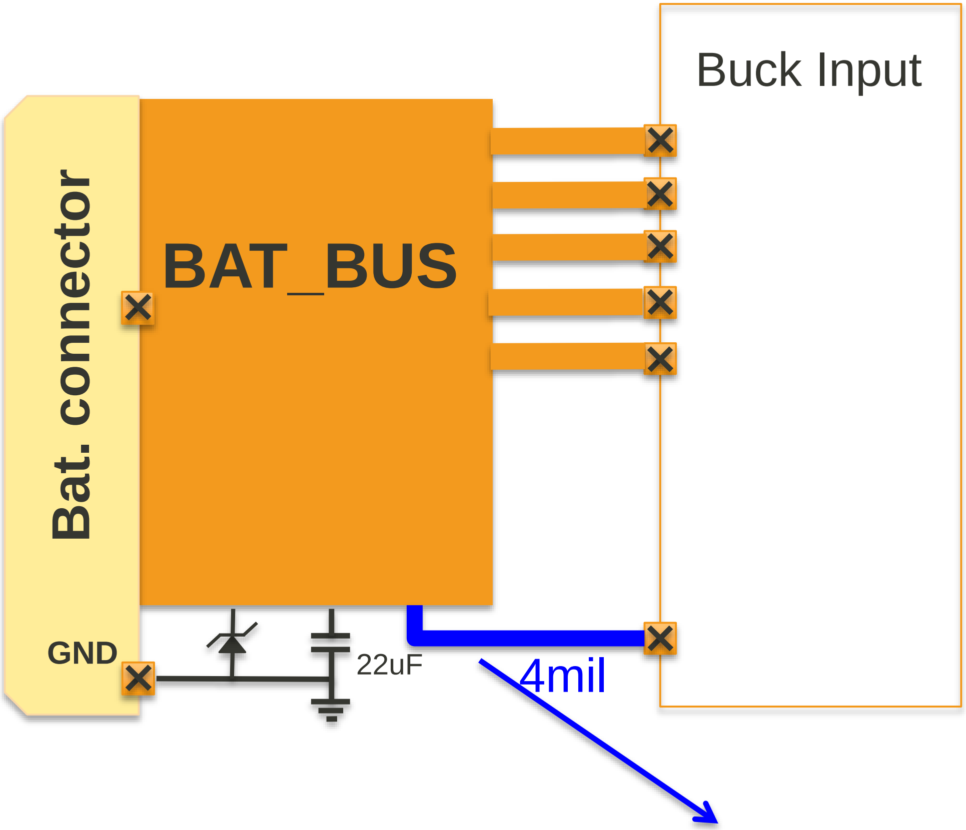
- Buck Power GND need to follow below description

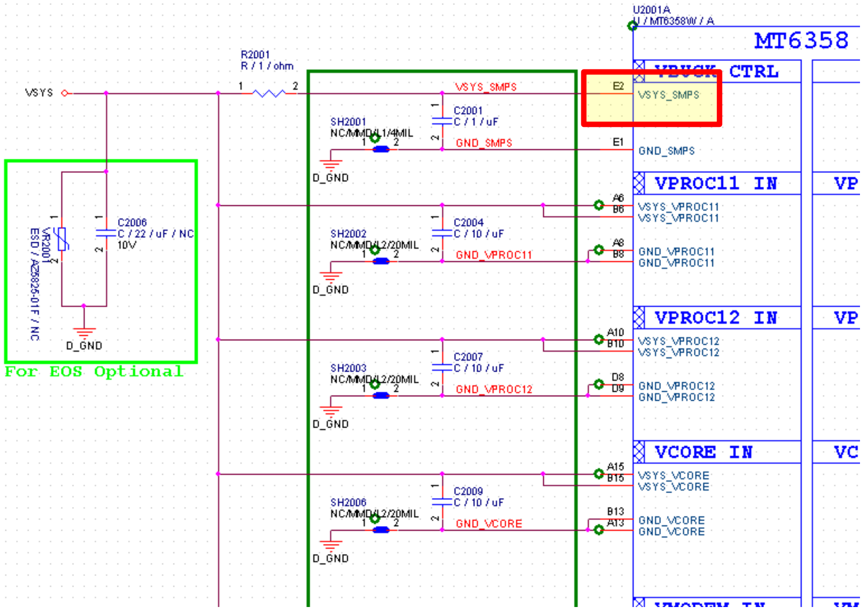


Note:
* Route ground return path as short as possible without fork (like the example "Bad routing", it isn't allowed)
** To connect buck ground to main ground, you can select either one (don't select multiple) of the three solutions.
solution 1 is the best, ground return from PMIC to input cap first, then connect to main ground.
solution 2 or 3 is also acceptable, but please note only diverge ground path underneath input cap ground is allowed.

Schematic/Layout Notice

Controller power trace layout constraint



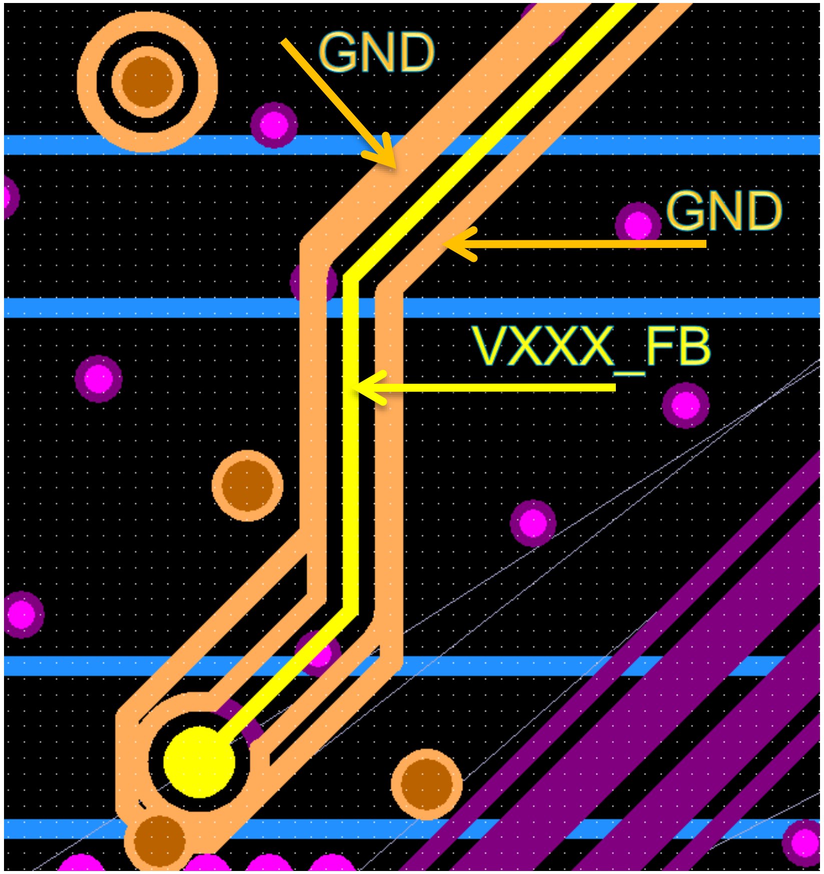


Buck controller power trace(VSYS_SMPS) must be use single trace connect to battery VBAT_BUS directly, and can't merge with others.
VSYS add 1Ω Resistor to VSYS_SMPS

Schematic/Layout Notice

Remote Sense Application Notice: Layout Guide (1)

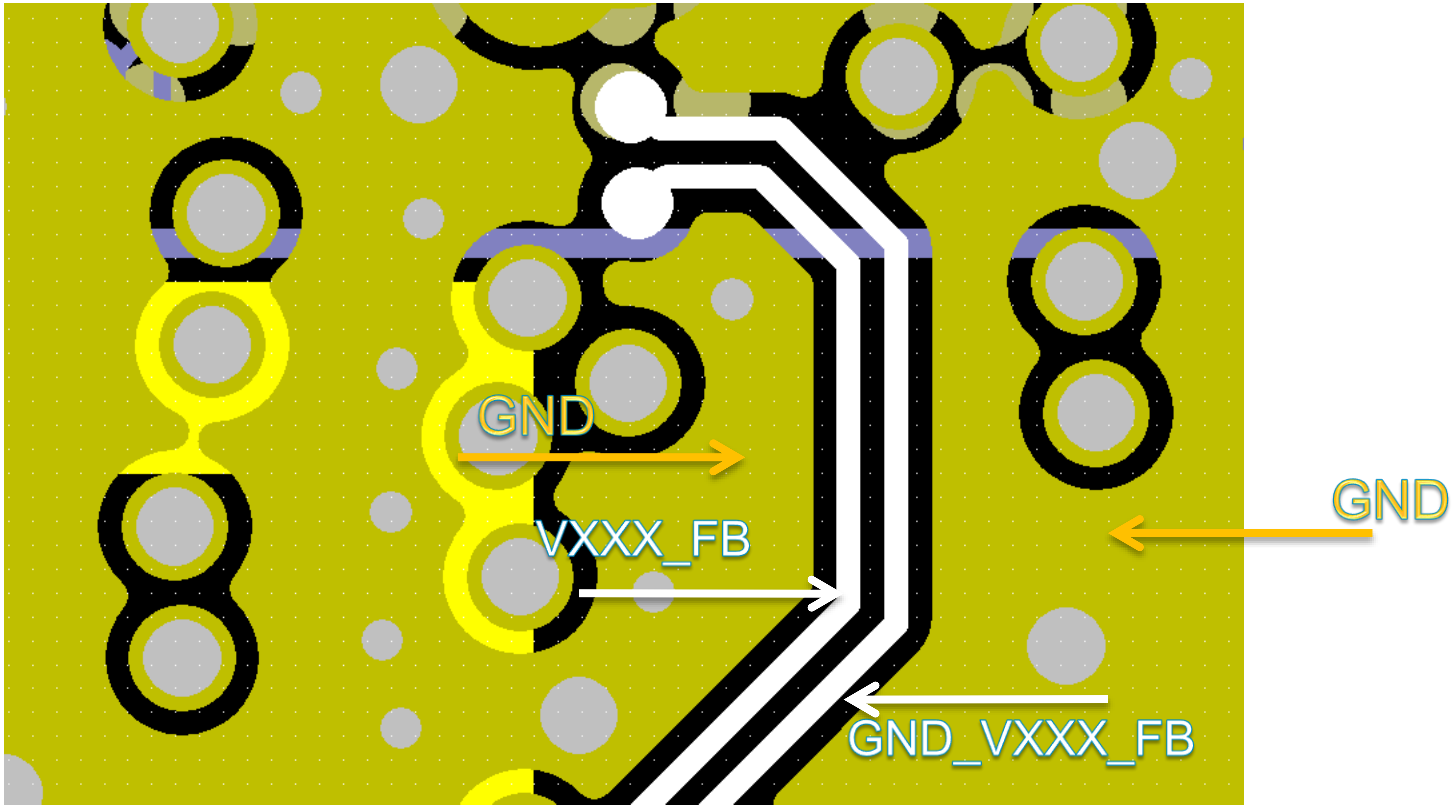
- DC/DC remote sense feedback traces are recommended using GND shielding to avoid noise coupled.



Schematic/Layout Notice

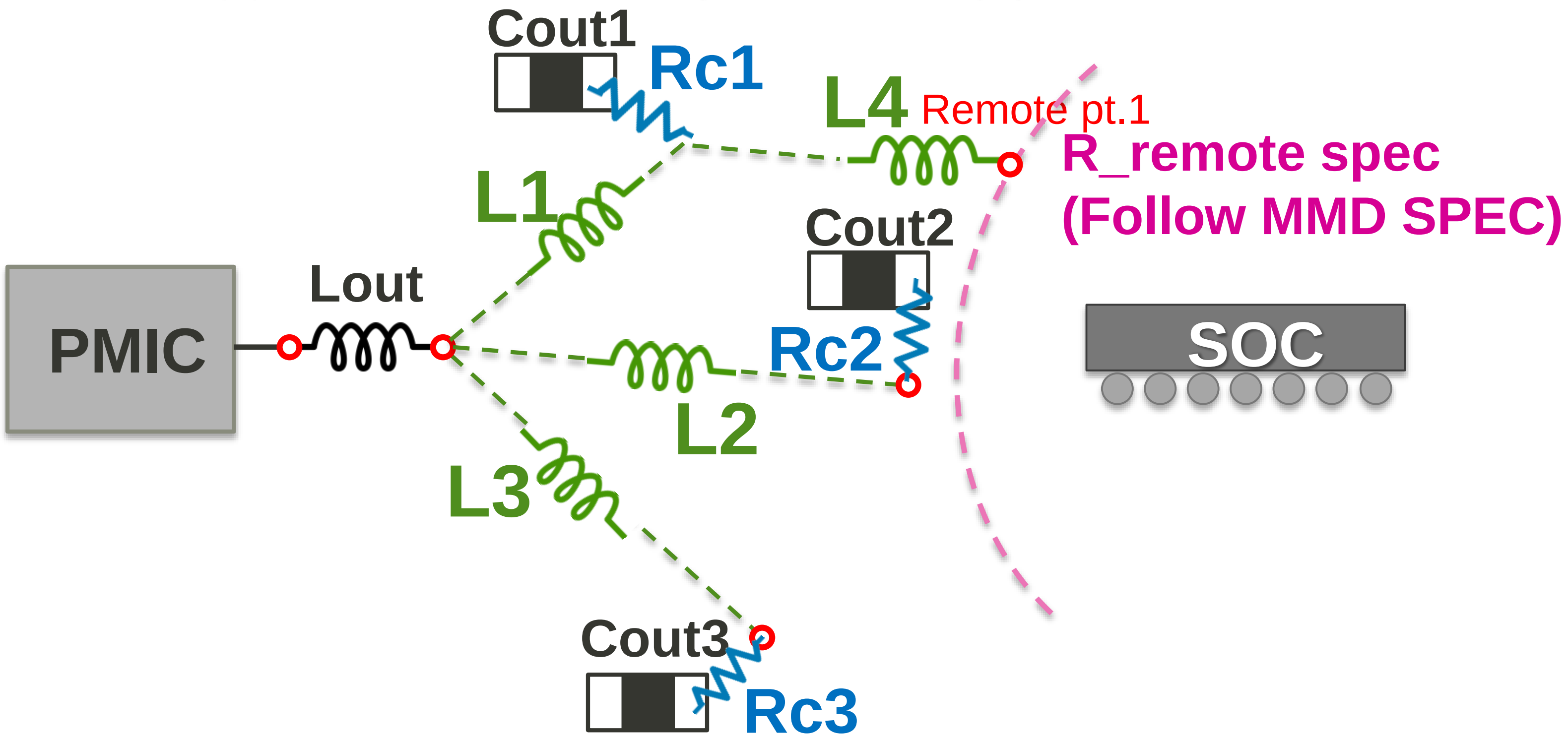
Remote Sense Application Notice: Layout Guide (2)

- DC/DC remote sense feedback & feedback_GND traces are recommended using GND shielding and differential pair to avoid noise coupled.



Schematic/Layout Notice

Remote Sense Application Notice: Layout Guide (3)

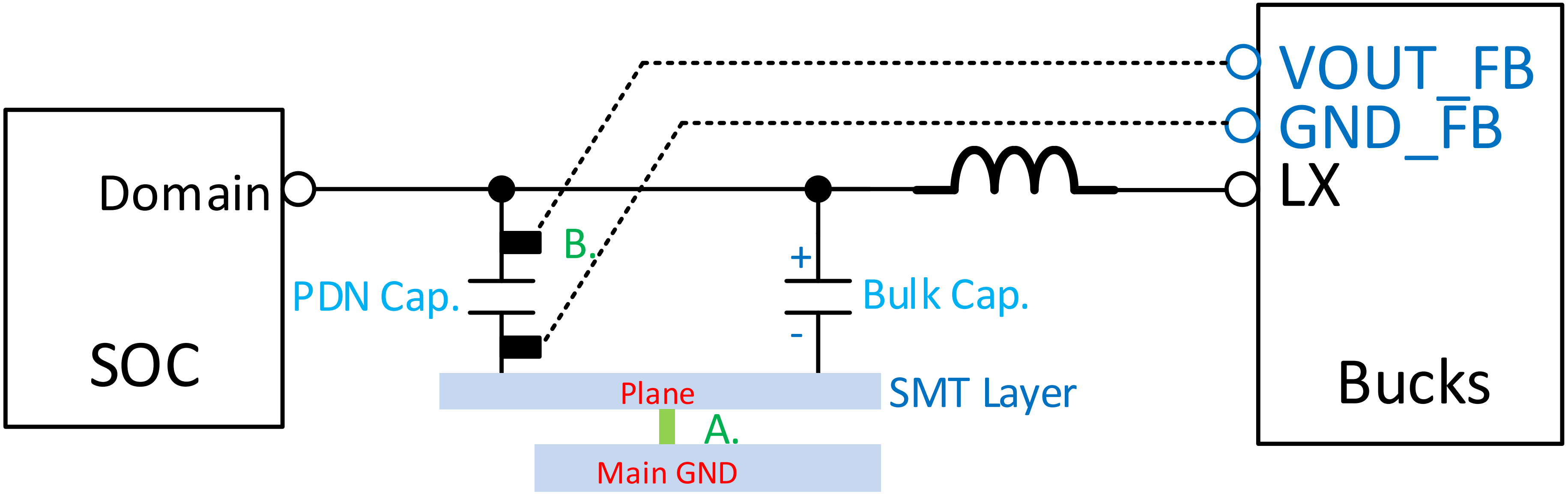


1. Find path with lowest inductance, the remote point can be located within $Cout_{lowest\ L}$ + 1n.
2. For example, in case of Cout1 is path with lowest inductance.
   - Inductance between Cout1 and Remote pt. 1 is L4, L4 must be lower than 1n (L4 < 1n).
   - The remote point location can be between Cout1 and Remote pt. 1.

3. Same case apply to L2 & L3 if they are lowest inductance path.
4. Above case is for multi-path, in case of single path, consider the only path as the lowest inductance path directly.

Schematic/Layout Notice

Remote Sense Application Notice: Layout Guide (4)



A. For GND/VOUT of PDN/Bulk cap. pads, please tie together through Plane before connected to Main GND.

B. GND_FB/VOUT_FB (Fully differentially connected) trace routes directly to PDN cap. pads through short-pad at the layer PDN cap. placed, which also satisfies "Remote Sense Application Notice : Layout Guide (3)"

Critical Component Selection Guide:

Buck Inductor Selection Guideline

- Inductors are recommended to follow below notice.
  1. Rate current of the inductor should be follow bellow table:

  (Inductance change within +/-30% from nominal value).

  2. Although small size and high efficiency are major concerns, the inductor should have low core losses and low DCR (copper wire resistance). Efficiency data in MT6358 datasheet is based on 30 mΩ DCR.

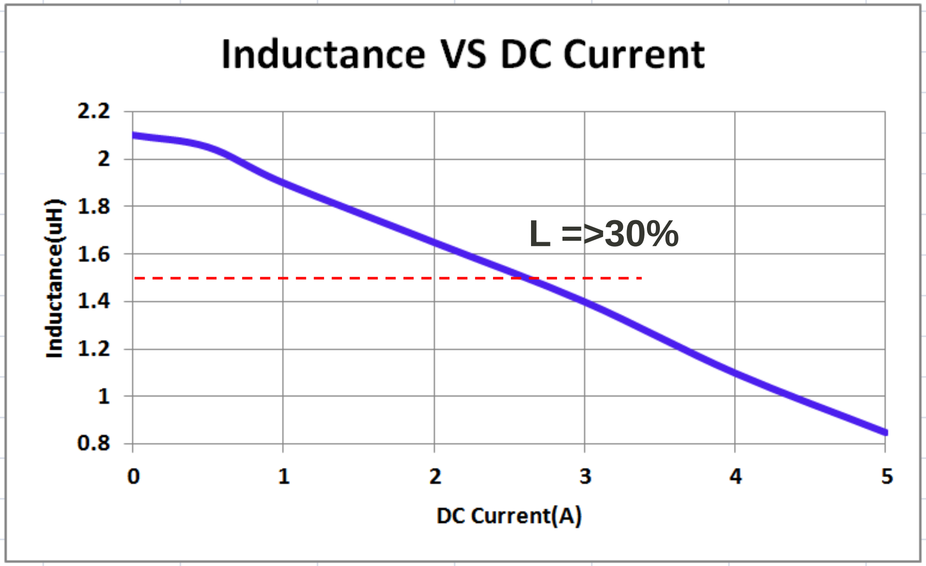
Note:Idc1: Depends on inductance saturation. (-30% reduction from Initial L value)

IP	Inductance	IDC1(A),MAX
VS1	1	2.6
VS2	1	2.5
VDRAM	1	2.5
VPA	1	4
VMODEM	1	4
VPROC11	0.47	5.3
VPROC12	0.47	3.85
VCORE	0.47	5.3
VGPU	0.47	3.9

for VPA IR Drop issue need check DCR< 82mohm @85C

Critical Component Selection Guide:
Inductor Selection Guideline

Example:



Note:

1. The inductor saturation current with 30% decreasing “must be” higher than PMIC Imax for all operation condition.

VPA PCB Layout Constraint

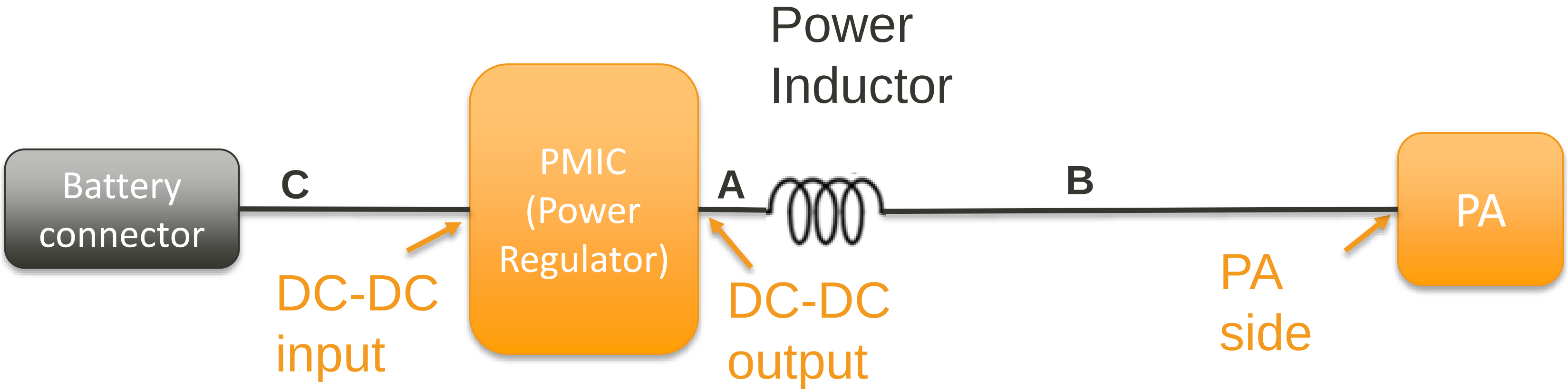
- Power Domain Information and PCB Layout Constraint

Power Domain	PA Min. Voltage(V)	Loading Current(A)	PCB Resistance A+B+C constraint(mΩ)
VPA	3.15@Vout3.4V	1.0	< 70

- Example of PCB Layout Constraint *1

Power Domain	PCB Resistance A+B+C constraint (mΩ)	PCB Width A+B+C (mil)	PCB Length A+B+C (mil)	Cu Thickness (OZ)
VPA	< 70	≥ 60	≤ 4000	0.5

***1**: Reduce the width acceptable at IC fan out , total PCB resistance need to meet constraint. Suggest the minimum width ≥ 20mils and length <100mils at IC fan out



Electrical Equations of PCB Resistance reference:
http://circuitcalculator.com/wordpress/2006/01/24/trace-resistance-calculator

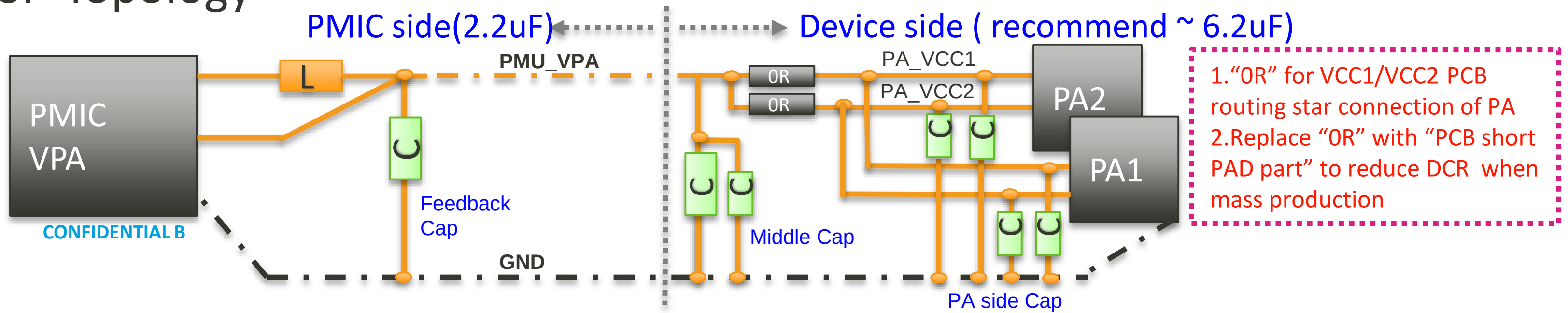
VPA Output Capacitance Notice(1)

- Why define the output capacitor range
  - The PA's transient voltage and timing are more critical
    - Stability ,ripple and transient voltage drop issue If output capacitor is too small
    - Stability and dynamic voltage scaling timing issue If output capacitor is too bigger
- Capacitor Specification Requirement
  - The updated is for dimension of capacitor don't care that accept small than 0603 and only need to follow the absolute effective capacitance shown below table. The electrical performance also be guarantee for the previous capacitance notice.
  - Typical total output capacitance is 2.2uF (Feedback)+ ~ 6.2uF (Middle +PA)

Item	Typical Cap(uF)	Effective Min Cap (uF) *1	Effective Max Cap (uF) *2	Rated V(V)	Placement Location
Feedback Cap	2.2	**0.7**	**X**	>=6.3	Close PMIC for PMIC FB sense pin
Feedback Cap+ (Middle +PA side Cap)	2.2+~6.2	**4.2**	**7.0**	>=6.3	Feedback Cap Close to PMIC ; Others Close to PAs.

*1 : -30°C~85°C / DC=0.5~3.6V / AC=0.01Vrms
*2 : -30°C~85°C / DC=2.5~3.6V / AC=0.01Vrms , the capacitance increased when lower DC

- Capacitor Topology



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VPA Output Capacitance Notice(2)

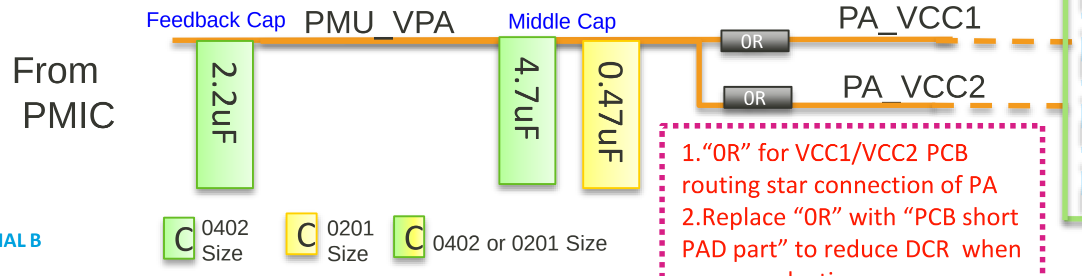
- Example for Capacitors arrangement

Example	Example 1 : PA side 0201 size		Example 2 : PA side 0402 size	
Location	1 PA – Cap/Size	2 PAs– Cap/Size	1 PA – Cap/Size	2 PAs– Cap/Size
PMIC FB Cap	2.2uF/0402	2.2uF/0402	2.2uF/0402	2.2uF/0402
Middle Cap	1. 4.7uF/0402 ; 2. 0.47uF/0201	1. 4.7uF/0402 ; 2. 0.47uF/0201	1. 4.7uF/0402 ; 2. NC/0201	1. 4.7uF/0402 ; 2. NC/0201
PAs side Cap	1. 0.47uF *3/0201 2. <=100pF *3/0201	1. 0.47uF *4/0201 2. <=100pF *4/0201	1. 0.47uF *3/0402 2. <=100pF *3/0201	1. 0.47uF *4/0402 2. <=100pF *4/0201

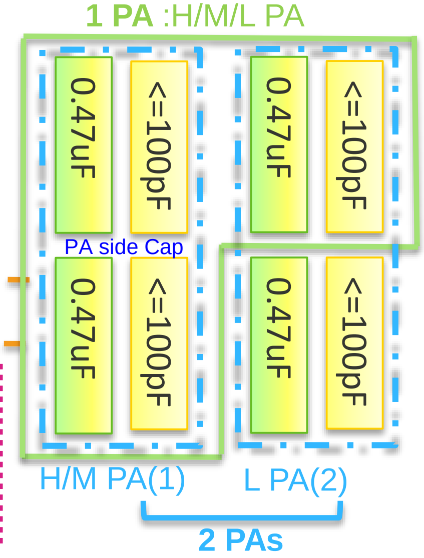
- Part Reference : http://ds.murata.co.jp/software/simsurfing/en-us/#

Part	Part Number	Rated Voltage(V)	Part Size
0.47uF	GRM033R60J474KE90	6.3	0201
0.47uF	GRM155R60J474ME19	6.3	0402
1.0uF	GRM155R60J105ME19	6.3	0402
2.2uF	GRM155R60J225ME95	6.3	0402
4.7uF	GRM155R61A475MEAA	10	0402

Cap. Topology



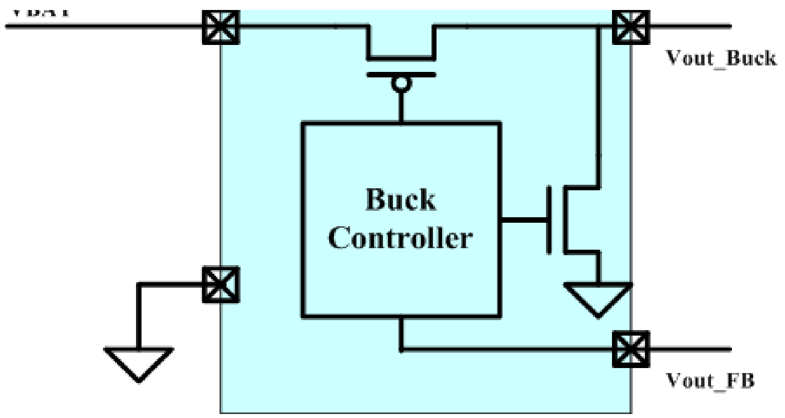
1."0R" for VCC1/VCC2 PCB routing star connection of PA
2.Replace "0R" with "PCB short PAD part" to reduce DCR when mass production



Reference Design

Buck Un-used configuration-VPA

- Configuration for VPA not in use:
  - VBAT_PA connect to VBAT
  - GND_PA connect to GND
  - VPA : floating
  - VPA_FB: floating
- Register setting
  - RG_VPA_EN = 0
  - RG_VPA_NDIS_EN = 1



LDO

LDO Constraint Outline

- LDO PCB Placement Rule
- LDO Capacitor Range
- LDO Layout Constraint
- VMCH Disable by HW_DET
- AP Analog Power PCB Layout Constrain

LDO PCB Placement Rule

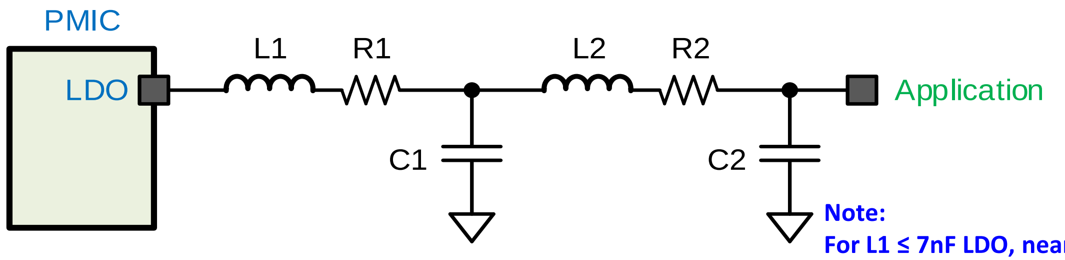
- If LDO is "default off" and loading current is 0mA, output capacitor can be removed.
- If VDRAM2 current rating is lower than 0.1mA, min capacitor can be reduced to 1uF.
- For the PCB LDO layout reference, please refer to the "MT6771 PCB Design Guidelines" "MT6358 LDO Output (1/2)"

LDO Capacitor Range

LDO Type	LDO Name	Cout Range
SLDO1	VRF18	9.4uF~10.4uF
SLDO2	VRF12	9.4uF~10.4uF
SLDO2	VDRAM2	22uF ~ 44uF
ALDO	VFE28	1uF ~ 2.2uF
DLDO	VEFUSE	1uF ~ 2.2uF
ALDO	VCN28	1uF ~ 2.2uF
DLDO	VUSB	1uF ~ 2.2uF
DLDO	VIBR	1uF ~ 2.2uF
ALDO	AUX18	1uF ~ 2.2uF
SLDO1	VCN18	1uF ~ 2.2uF
ALDO	VXO22	2.2uF ~ 2.3uF
DLDO	VMC	1uF ~ 2.2uF
ALDO	VAUD28	1uF ~ 2.2uF
SLDO2	VSRAM_PROC11	2.2uF ~ 3.61uF
SLDO2	VSRAM_PROC12	2.2uF ~ 3.61uF
SLDO2	VSRAM_GPU	2.2uF ~ 3.61uF
SLDO2	VSRAM_OTHERS	2.2uF ~ 3.61uF
DLDO	VSIM1	1uF ~ 2.2uF
DLDO	VSIM2	1uF ~ 2.2uF
DLDO	VCN33	1uF ~ 5.7uF
DLDO	VMCH	1uF ~ 5.9uF
DLDO	VEMC	1uF ~ 5.9uF
DLDO	VIO28	1uF ~ 11.5uF
SLDO1	VIO18	10uF ~ 30uF
ALDO	VCAMA1	1uF ~ 21uF
ALDO	VCAMA2	1uF ~ 21uF
SLDO1	VCAMD	For CAMD : 5.7uF ~ 25uF
		For VA09 : 4.7uF ~ 25uF
SLDO1	VCAMIO	1uF ~ 4uF
DLDO	VLDO28	1uF ~ 7.7uF
ALDO	VBIF28	1uF ~ 2.2uF
SLDO1	VA12	2.2uF ~ 4.84uF
DVDD18	DVDD18_DIG	1uF
VRTC	VRTC28	Near end: C: 0.1uF Far end: R 1.5k + super cap

Layout Constraint #1

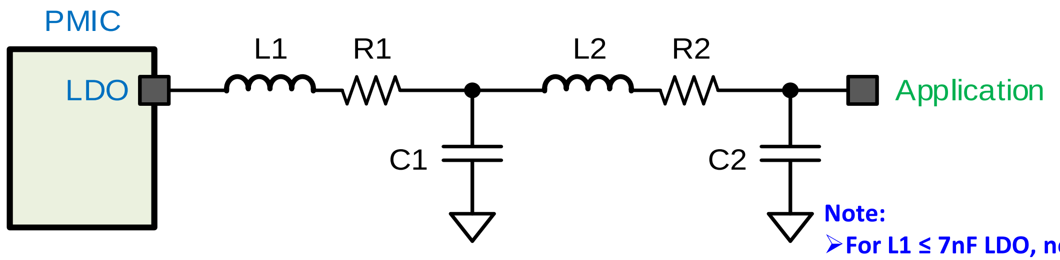
LDO Layout Constraint for Stability								
LDO	**L1 ≤**	**R1≤**	**C1 Minimum**	**C1+C2 Minimum**	**(L1+L2)≤**	**(R1+R2)≤**	**C2 Maximum**	**Maximum Cap**
VRF18	7nH	0.2Ω	4.7uF	9.4uF	27nH	0.4Ω	5.7uF	10.4uF
VRF12	7nH	0.2Ω	4.7uF	9.4uF	27nH	0.4Ω	5.7uF	10.4uF
VSRAM_PROC11	7nH	0.2Ω	2.2uF	2.2uF	27nH	0.4Ω	1.41uF	3.61uF
VSRAM_PROC12	7nH	0.2Ω	2.2uF	2.2uF	27nH	0.4Ω	1.41uF	3.61uF
VSRAM_OTHERS	7nH	0.2Ω	2.2uF	2.2uF	27nH	0.4Ω	1.41uF	3.61uF
VSRAM_GPU	7nH	0.2Ω	2.2uF	2.2uF	27nH	0.4Ω	1.41uF	3.61uF
VIO18	7nH	0.2Ω	4.7uF	10uF	27nH	0.6Ω	25.3uF	30uF
VCN33	7nH	0.2Ω	1uF	1uF	27nH	0.4Ω	4.7uF	5.7uF
VMCH	7nH	0.2Ω	1uF	1uF	27nH	0.4Ω	4.7uF	5.7uF
VEMC	7nH	0.2Ω	1uF	1uF	27nH	0.32Ω	4.9uF	5.9uF



Note:
For L1 ≤ 7nF LDO, near-end Cap C1 can be removed if meet bellow spec.
Take VEMC as example: Near-end cap can be removed
If trace's inductive reactance ≤ 7nH, impedance ≤ 0.2Ω.
VEMC's inductive reactance should within 27nH, impedance within 0.32Ω.

Layout Constraint #2

LDO Layout Constraint for Stability							
LDO	L1 ≤	R1≤	C1 Minimum	(L1+L2)≤	(R1+R2)≤	C2 Maximum	Maximum Cap
VIO28	7nH	0.2Ω	1uF	27nH	0.6Ω	10.5uF	11.5uF
VSIM1	7nH	0.2Ω	1uF	27nH	0.6Ω	1.2uF	2.2uF
VSIM2	7nH	0.2Ω	1uF	27nH	0.6Ω	1.2uF	2.2uF
VDRAM2	7nH	16mΩ	1uF	7nH	16mΩ	43uF	44uF
VFE28	20nH	0.2Ω	1uF	40nH	0.4Ω	1.2uF	2.2uF
VEFUSE	20nH	0.2Ω	1uF	40nH	0.4Ω	1.2uF	2.2uF
VCN28	20nH	0.2Ω	1uF	40nH	0.4Ω	1.2uF	2.2uF
VUSB	20nH	0.2Ω	1uF	40nH	0.4Ω	1.2uF	2.2uF
VBIF28	20nH	0.2Ω	1uF	40nH	0.4Ω	1.2uF	2.2uF



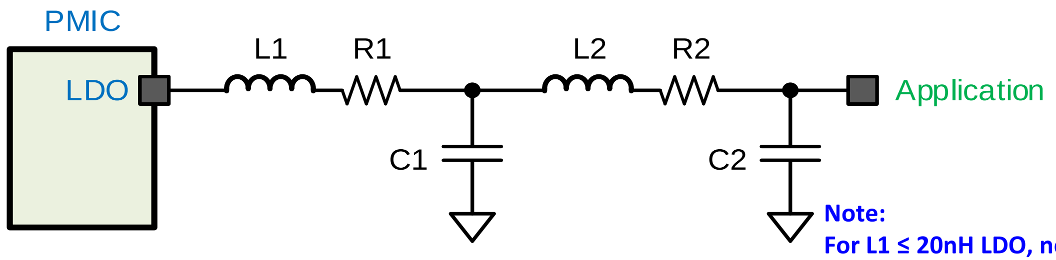
Note:

➢For L1 ≤ 7nF LDO, near-end Cap C1 can be removed if meet bellow spec.
Take VIO28 as example: Near-end cap can be removed
If trace's inductive reactance ≤ 7nH, impedance ≤ 0.2Ω.
VIO28's inductive reactance should within 27nH, impedance within 0.6Ω.

➢For L1 ≤ 20nH LDO, near-end Cap C1 can be removed if meet bellow spec.
Take VCN28 as example: Near-end cap can be removed
If trace's inductive reactance ≤ 20nH, impedance ≤ 0.2Ω.
VCN28's inductive reactance should within 40nH, impedance should within 0.4Ω.

Layout Constraint #3

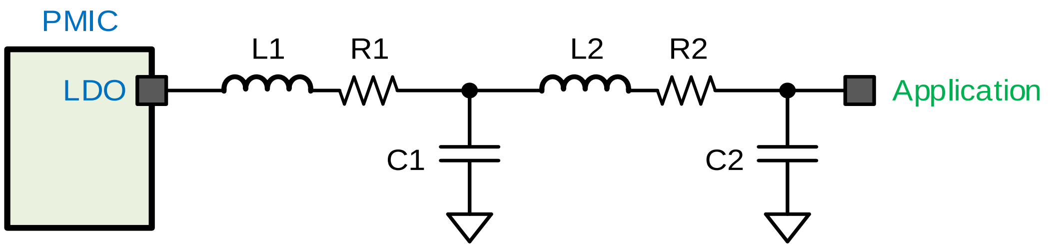
LDO Layout Constraint for Stability							
LDO	**L1 ≤**	**R1≤**	**C1 Minimum**	**(L1+L2)≤**	**(R1+R2)≤**	**C2 Maximum**	**Maximum Cap**
VIBR	20nH	0.2Ω	1uF	40nH	0.4Ω	1.2uF	2.2uF
VRTC	20nH	0.2Ω	0.1uF	20nH	0.2Ω	R:1.5k + C: Super Cap	NA
DVDD18_DIG	20nH	0.2Ω	1uF	20nH	0.2Ω	0uF	1uF
VAUX18	20nH	0.2Ω	1uF	40nH	0.4Ω	1.2uF	2.2uF
VCN18	20nH	0.2Ω	1uF	40nH	0.4Ω	1.2uF	2.2uF
VA12	20nH	0.2Ω	2.2uF	40nH	0.4Ω	2.64uF	4.84uF
VXO22	20nH	0.2Ω	2.2uF	40nH	0.4Ω	0.1uF	2.3uF
VLDO28	20nH	0.2Ω	1uF	40nH	0.4Ω	6.7uF	7.7uF



Note:
For L1 ≤ 20nH LDO, near-end Cap C1 can be removed if meet bellow spec.
Take VCN18 as example: Near-end cap can be removed
if trace's inductive reactance ≤ 20nH, impedance ≤ 0.2Ω.
VCN18's inductive reactance should within 40nH, impedance should within 0.4Ω.

Layout Constraint #4

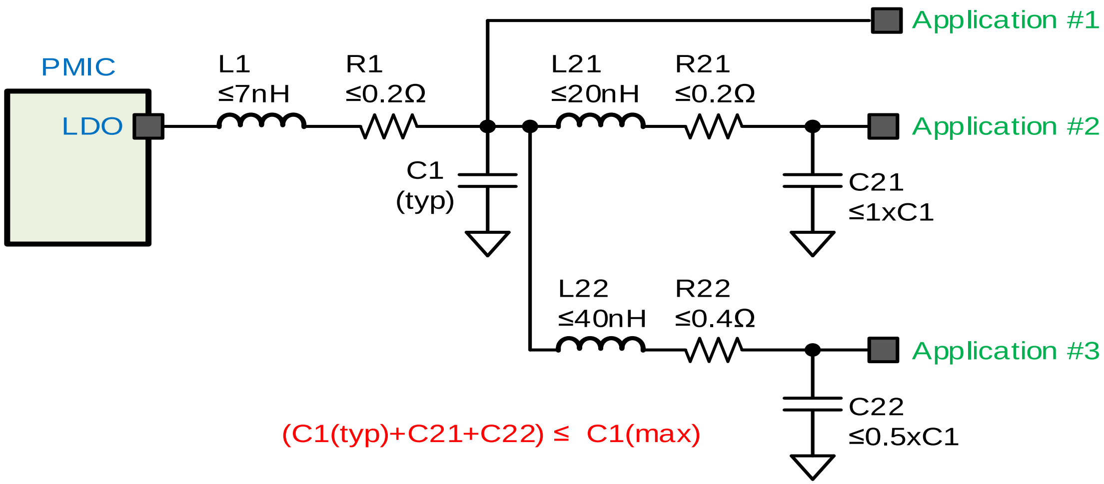
LDO Layout Constraint for Stability								
LDO	L1 ≤	R1≤	C1 Minimum	C1+C2 Minimum	(L1+L2)≤	(R1+R2)≤	C2 Maximum	Maximum Cap
VMC	20nH	0.2Ω	1uF	1uF	40nH	0.4Ω	1.2uF	2.2uF
VAUD28	20nH	0.2Ω	1uF	1uF	40nH	0.4Ω	1.2uF	2.2uF
VCAMA1	20nH	0.2Ω	1uF	1uF	40nH	0.4Ω	20uF	21uF
VCAMA2	20nH	0.2Ω	1uF	1uF	40nH	0.4Ω	20uF	21uF
VCAMD	20nH	0.2Ω	2.2uF	5.7uF	40nH	0.4Ω	22.8uF	25uF
VCAMIO	20nH	0.2Ω	1uF	1uF	40nH	0.4Ω	3uF	4uF



Note:
For L1 ≤ 20nH LDO, near-end Cap C1 can be removed if meet bellow spec.
Take VMC as example: Near-end cap can be removed
if trace's inductive reactance ≤ 20nH, impedance ≤ 0.2Ω.
VMC's inductive reactance should within 40nH, impedance should within 0.4Ω.

Layout Constraint #5

- Multi-application Notice
  - Typical cap please refer design notice
  - DC spec is no included PCB DC drop
  - Each trace width > 6mil
- Below LDOs can't follow this common rule
  - VSRAM_xxx
  - VRF12, VRF18, VDRAM, VMCH, VIO18, VIO28, VCAMA, VCAMD



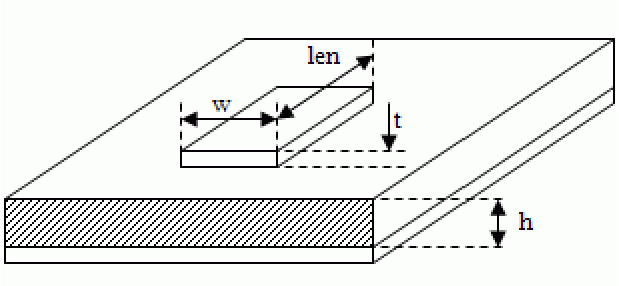
Rough Guidelines-use from CAD Extraction

w (mil)	w (um)	h (um)	t @ 1/3 oz (um)	len (cm)	trace inductance (nH)	trace resistance (mΩ)
4	101.6	50	12	1.27	4.85	198

$$L\,(\text{nH}) = 4.85\text{ nH} \times \frac{101.6\text{ um}}{w} \times \frac{len}{1.27\text{ cm}}$$

$$R\,(\text{m}\Omega) = 198\text{ m}\Omega \times \frac{101.6\text{ um}}{w} \times \frac{len}{1.27\text{ cm}}$$

where w = 4mil~40mil

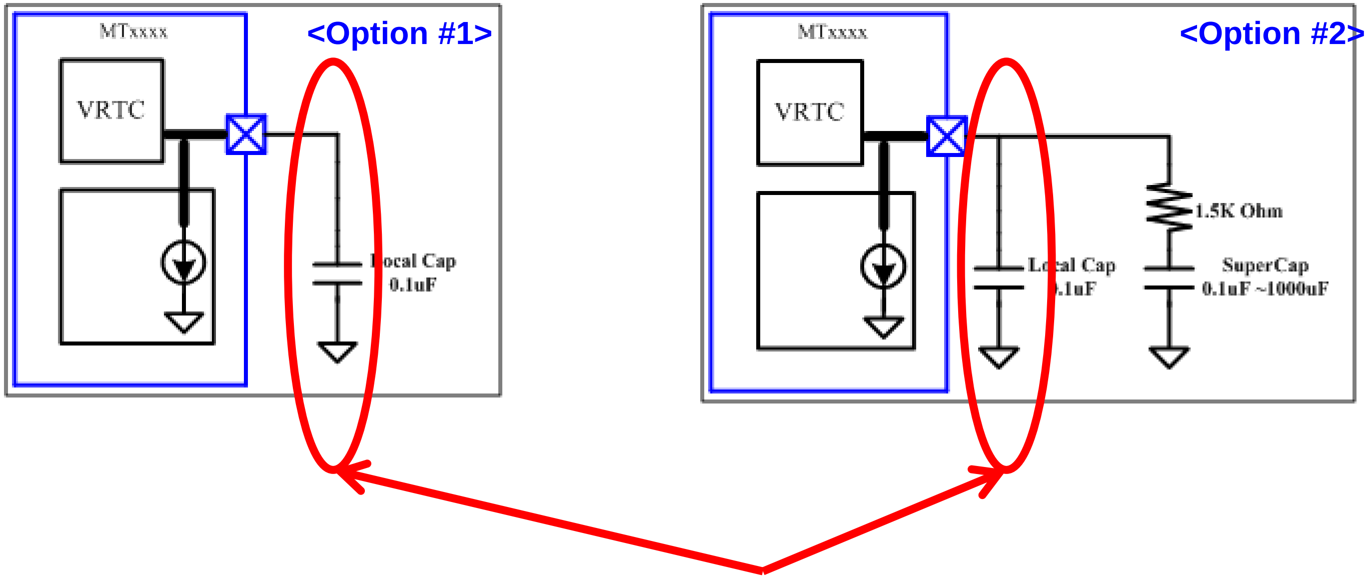


Parameter	Value
Dielectrically constant	4.0
Conductivity	5.8e7 s/m

w = trace width
len = trace length
t = trace thickness
h = dielectric height

Layout Constraint of VRTC

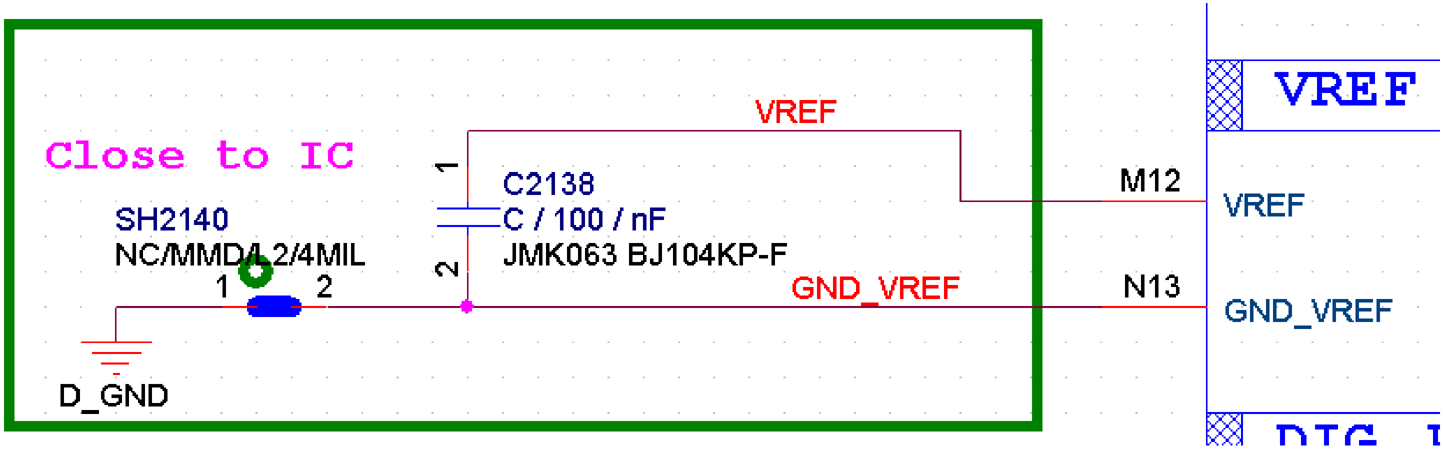
- VRTC: Application circuit (2 options)
  - <Option #1> 0.1uF
  - <Option #2> 0.1uF + 1.5kΩ + super cap



0.1uF cap MUST and be close to PMIC

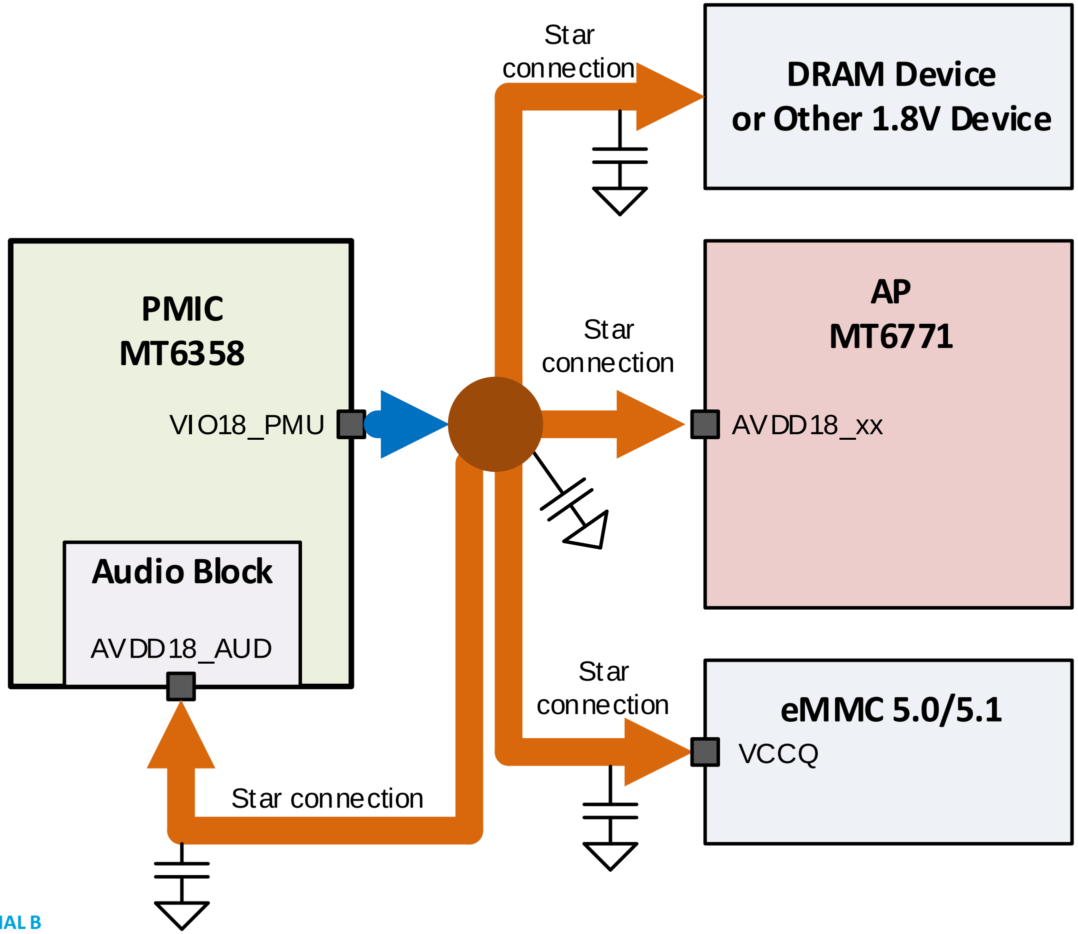
Layout Constraint of VREF

- VREF bypass cap as close as possible to PMIC
- GND_VREF pin must first connect to capacitor GND pin and then connect to system GND by VIA
- VREF cap is 0.1uF.



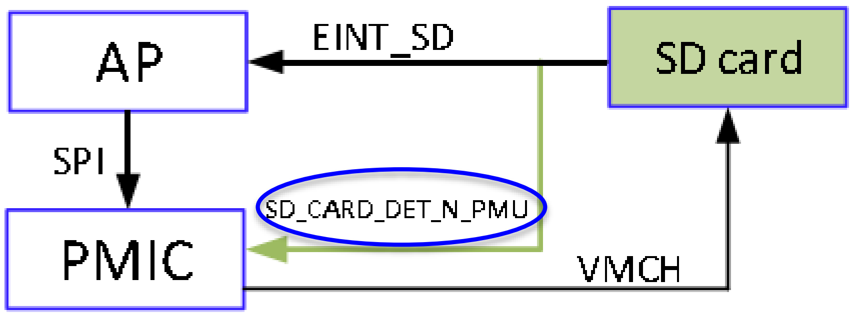
Layout Constraint of VIO_1V8

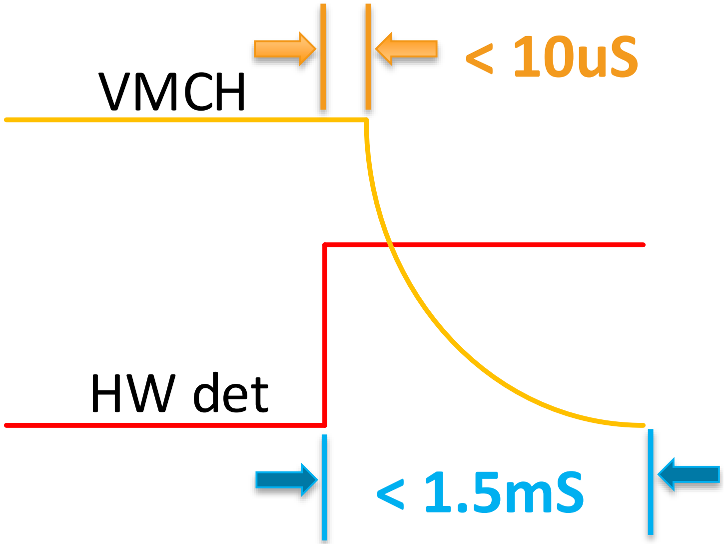
- Keep star-connection from PMIC VIO18_PMU to import 1.8V power domain.



VMCH Disable by HW

- Function Description
  - PMIC HW_DET(VREQ) to check the EINT_SD
  - HW_DET could configure as High/ Low active by register
  - HW_DET could control VMCH, VSIM1 and VSIM2 and setting by register
  - All function default off and controlled by “PMIC init setting”
- Spec
  - Reaction timing< 10us
  - SD card from plug out to VMCH= 1.8V < 0.3mS
  - SD card from plug out to VMCH off <1.5ms





AP ANALOG POWER PCB LAYOUT CONSTRAIN

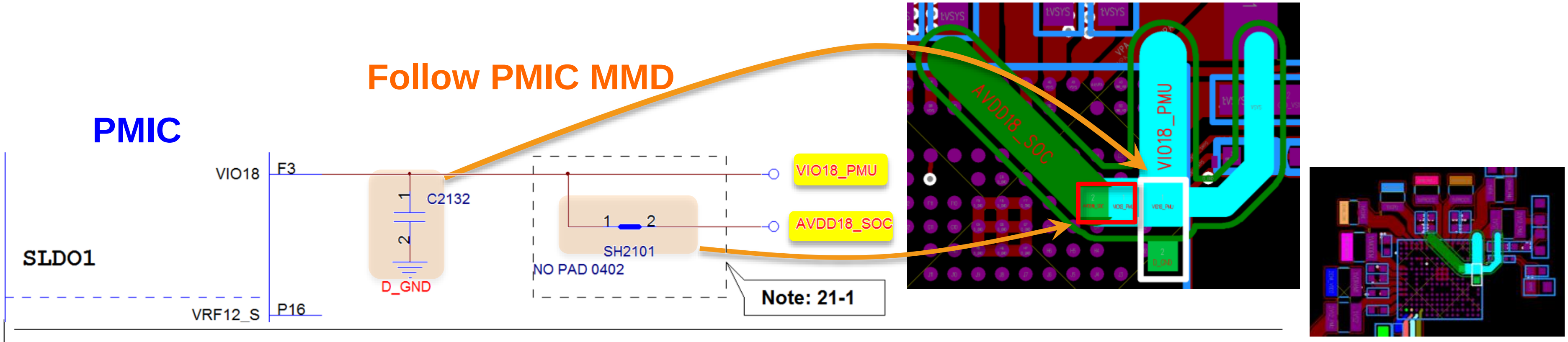
AP Analog and Power List

Voltage	PMIC Pin Name	Group#1 (AP analog pin name)	Group#2 (AP analog pin name)
1.8V	VIO18	AVDD18_MD, AVDD18_AP, AVDD18_WBG	AVDD18_USB, AVDD18_SSUSB, AVDD18_UFS, AVDD18_PLLGP
1.2V	VA12	AVDD12_MD, AVDD12_DSI, AVDD12_USB, AVDD12_UFS,	AVDD12_CSI, AVDD12_PLLGP, AVDD12_WBG
0.9V	VA09	AVDD09_UFS, AVDD09_SSUSB	N/A
3.075V	VUSB	AVDD33_USB	N/A

AP Analog Layout Constraint

AVDD18_xxx layout constraint

- **Star-connection** analog power group, **AVDD18_SOC by short-pad on VIO18 cap.**
- Please be sure to follow **"reference design" & "PMIC MMD"**



Schematic design notice of "21_POWER_MT6358-LDO" page.

Note 21-1: Please set SH2101 close to C2132, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132
Please also refer to MT6358 design notice for further detail design information

IR spec.

- **Total path from PMIC LDO pin to AVDD power pin of AP-site**
- **Target IR < 1%**
  - **For each AVDDXX_XXX path**
  - **Simulate all power pin currents at the same time**

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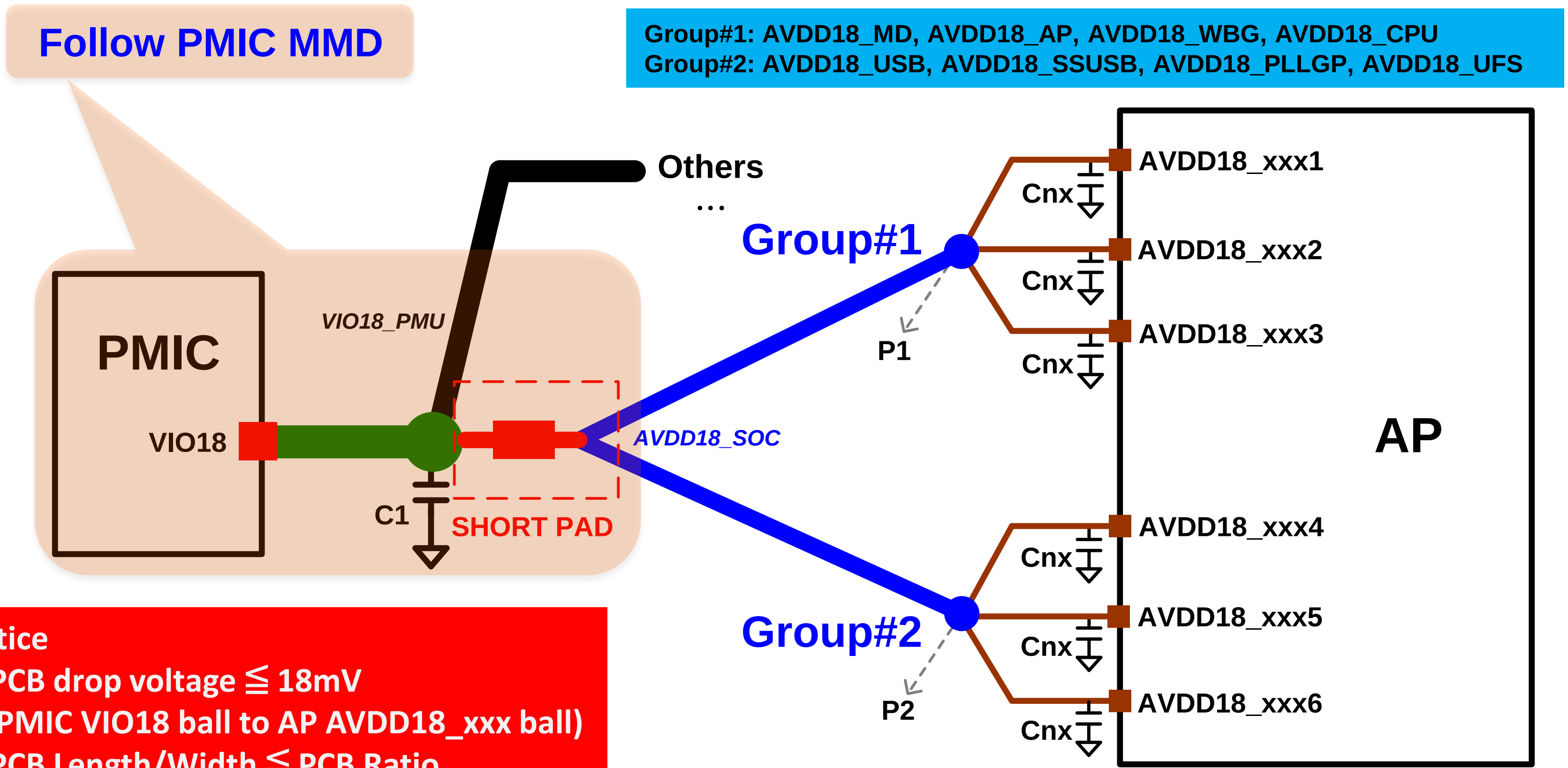
AP AVDD18_xxx Layout Guideline 1

Group#1: AVDD18_MD, AVDD18_AP, AVDD18_WBG, AVDD18_CPU
Group#2: AVDD18_USB, AVDD18_SSUSB, AVDD18_PLLGP, AVDD18_UFS



Notice
1. PCB drop voltage ≦ 18mV
   (PMIC VIO18 ball to AP AVDD18_xxx ball)
2. PCB Length/Width ≦ PCB Ratio

	Example		Average current	PCB Width	PCB Length	PCB Ratio Length/Width	PCB Thickness	PCB Resister	PCB drop voltage
Trace	Trace Start	Trace End							
Trace 1	PMIC VIO18 ball	C1	0.600A	20mil	180mil	9	0.3oz	16.0m	9.6mV
Trace 2	C1	P1/P2	0.080A	20mil	1000mil	50	0.3oz	88.7m	7.1mV
Trace 3	P1/P2	AP AVDD18_XXX ball	0.030A	12mil	300mil	25	0.3oz	44.3m	1.3mV

Pass ≦18mV

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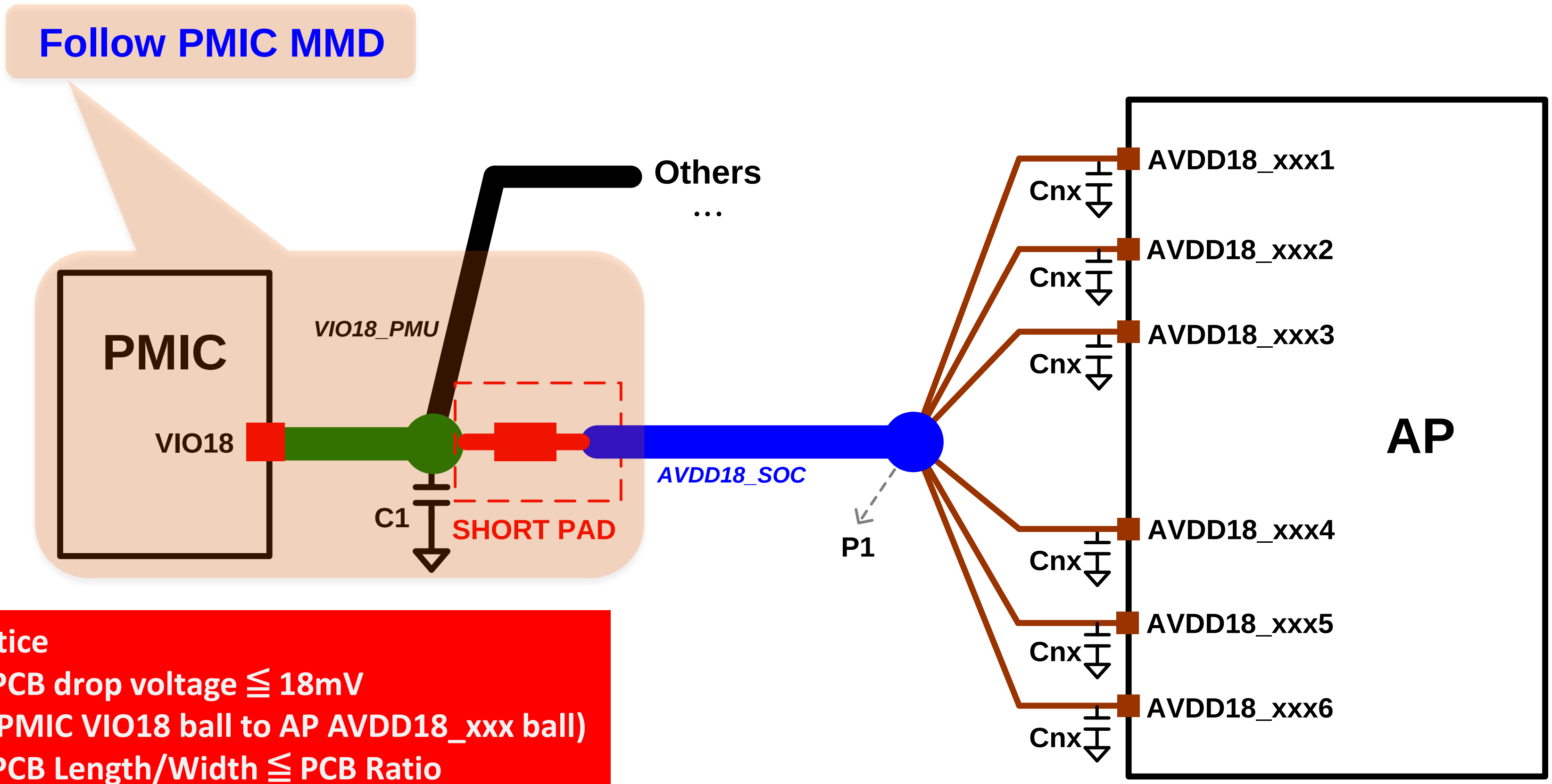
AP AVDD18_xxx Layout Guideline 2



Notice

1. PCB drop voltage ≦ 18mV
   (PMIC VIO18 ball to AP AVDD18_xxx ball)
2. PCB Length/Width ≦ PCB Ratio

	Example		Average current	PCB Width	PCB Length	PCB Ratio Length/Width	PCB Thickness	PCB Resister	PCB drop voltage
Trace	Trace Start	Trace End							
Trace 1	PMIC VIO18 ball	C1	0.600A	20mil	180mil	9	0.3oz	16.0m	9.6mV
Trace 2	C1	P1	0.150A	42mil	1100mil	26	0.3oz	46.5m	7.0mV
Trace 3	P1	AP AVDD18_XXX ball	0.030A	12mil	300mil	25	0.3oz	44.3m	1.3mV

Pass
≦18mV

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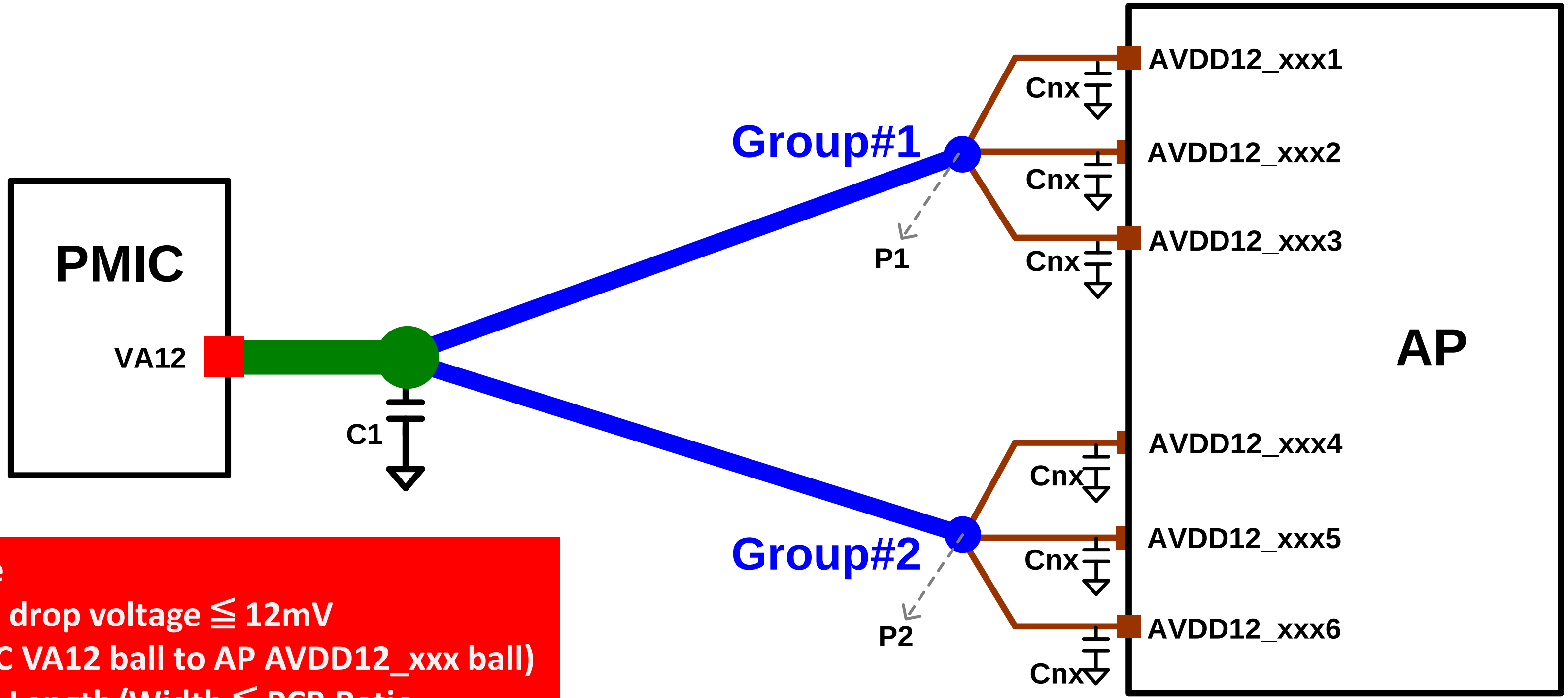
AP AVDD12_xxx Layout Guideline 1

Group#1: AVDD12_MD, AVDD12_DSI, AVDD12_USB, AVDD12_UFS
Group#2: AVDD12_CSI, AVDD12_PLLGP, AVDD12_WBG



Notice
1. PCB drop voltage ≦ 12mV
 (PMIC VA12 ball to AP AVDD12_xxx ball)
2. PCB Length/Width ≦ PCB Ratio

	Example		Average current	PCB Width	PCB Length	PCB Ratio Length/Width	PCB Thickness	PCB Resister	PCB drop voltage
Trace	Trace Start	Trace End							
Trace 1	PMIC VA12 ball	C1	0.120A	20mil	240mil	12	0.3oz	21.3m	2.6mV
Trace 2	C1	P1/P2	0.060A	16mil	1000mil	63	0.3oz	110.9m	6.7mV
Trace 3	P1/P2	AP AVDD12_XXX ball	0.040A	8mil	300mil	38	0.3oz	66.5m	2.7mV

Pass ≦12mV

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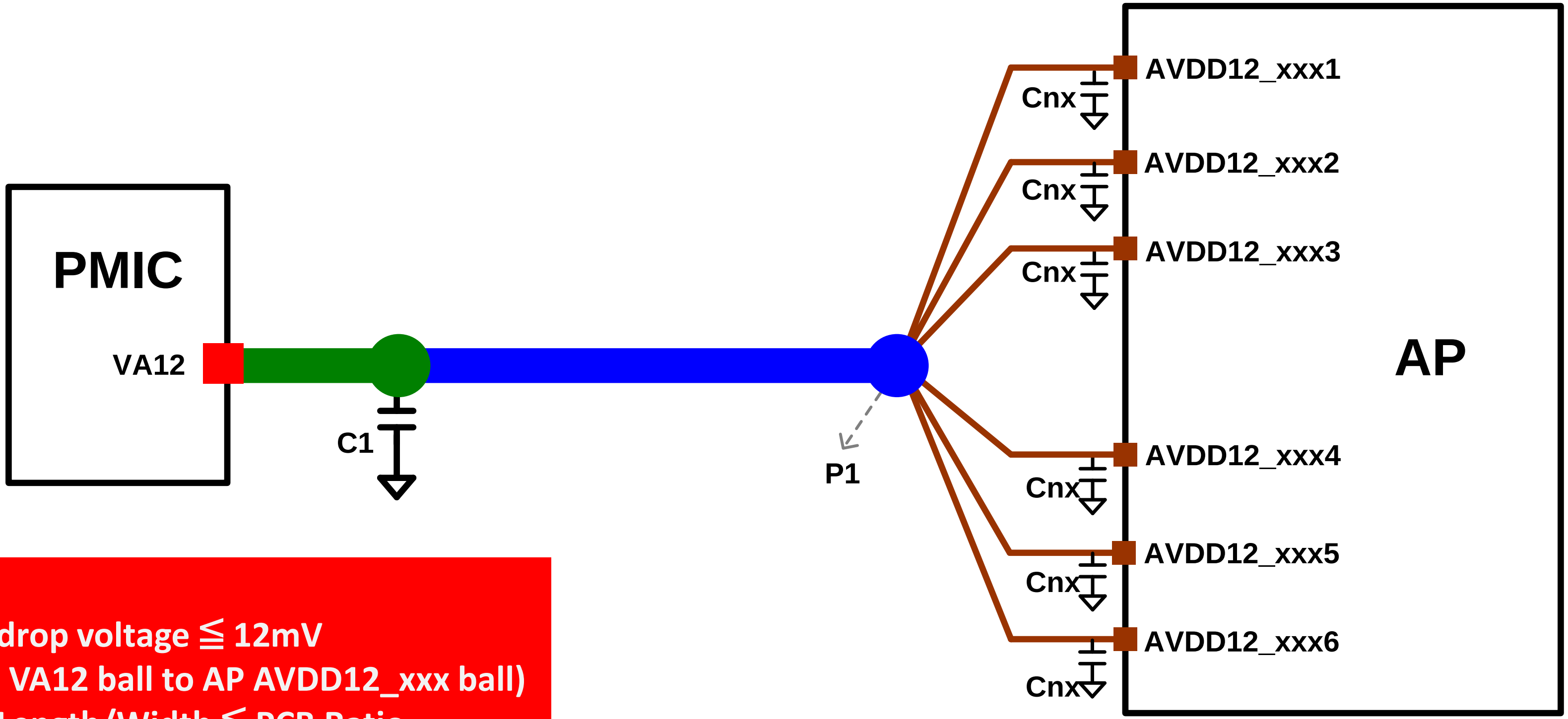
AP AVDD12_xxx Layout Guideline 2



Notice

1. PCB drop voltage ≦ 12mV
   (PMIC VA12 ball to AP AVDD12_xxx ball)
2. PCB Length/Width ≦ PCB Ratio

	Example		Average current	PCB Width	PCB Length	PCB Ratio Length/Width	PCB Thickness	PCB Resister	PCB drop voltage
Trace	Trace Start	Trace End							
Trace 1	PMIC VA12 ball	C1	0.120A	20mil	240mil	12	0.3oz	21.3m	2.6mV
Trace 2	C1	P1	0.120A	32mil	1000mil	31	0.3oz	55.4m	6.7mV
Trace 3	P1	AP AVDD12_XXX ball	0.040A	8mil	300mil	38	0.3oz	66.5m	2.7mV

Pass ≦12mV

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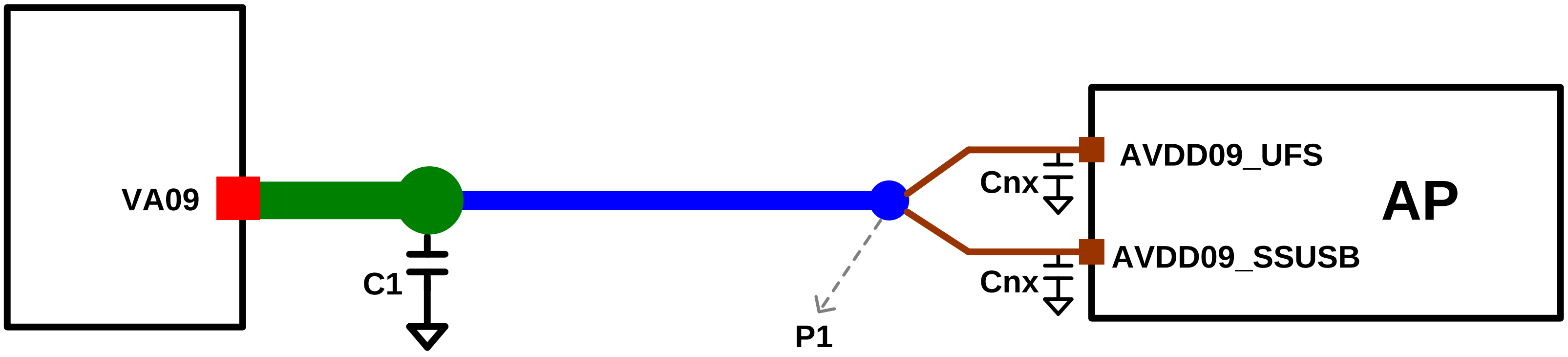
AP AVDD09_xxx Layout Guideline



Notice
1. PCB drop voltage ≦ 9mV
 (VA09 ball to AP AVDD09_xxx ball)
2. PCB Length/Width ≦ PCB Ratio

	Example		Average current	PCB Width	PCB Length	PCB Ratio Length/Width	PCB Thickness	PCB Resister	PCB drop voltage
Trace	Trace Start	Trace End							
Trace 1	VA09 ball	C1	0.060A	18mil	200mil	11	0.3oz	19.7m	1.2mV
Trace 2	C1	P1	0.060A	18mil	1000mil	56	0.3oz	98.5m	5.9mV
Trace 3	P1	AP AVDD09_XXX ball	0.040A	8mil	200mil	25	0.3oz	44.3m	1.8mV

Pass ≦9mV

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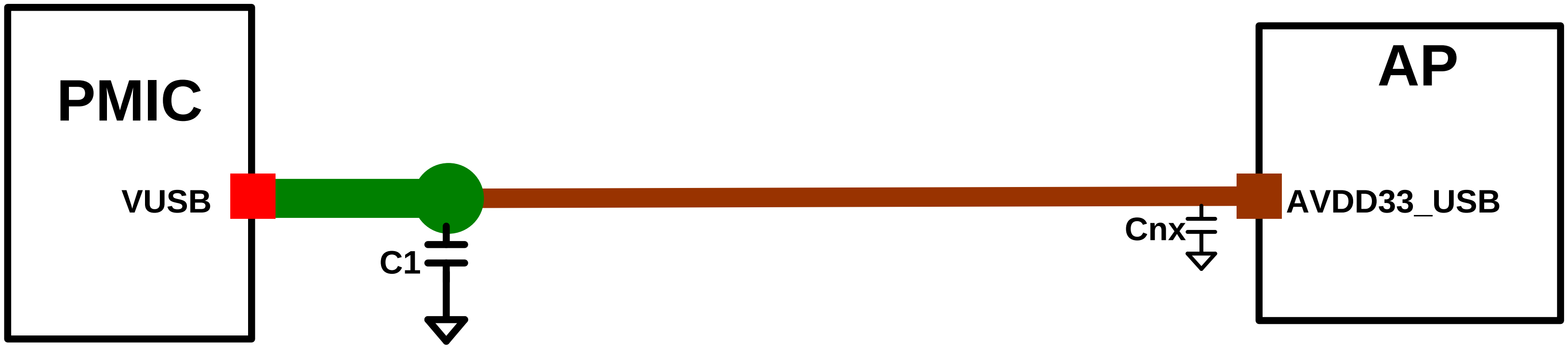
AP AVDD33_USB Layout Guideline



Notice
1. PCB drop voltage ≦ 30mV
(PMIC VUSB ball to AP AVDD33_USB ball)
2. PCB Length/Width ≦ PCB Ratio

	Example		Average current	PCB Width	PCB Length	PCB Ratio Length/Width	PCB Thickness	PCB Resister	PCB drop voltage
Trace	Trace Start	Trace End							
Trace 1	PMIC VUSB ball	C1	0.050A	8mil	200mil	25	0.3oz	44.3m	2.2mV
Trace 2	C1	AP AVDD33_USB ball	0.050A	8mil	2500mil	313	0.3oz	554.3m	27.7mV

Pass ≦30mV

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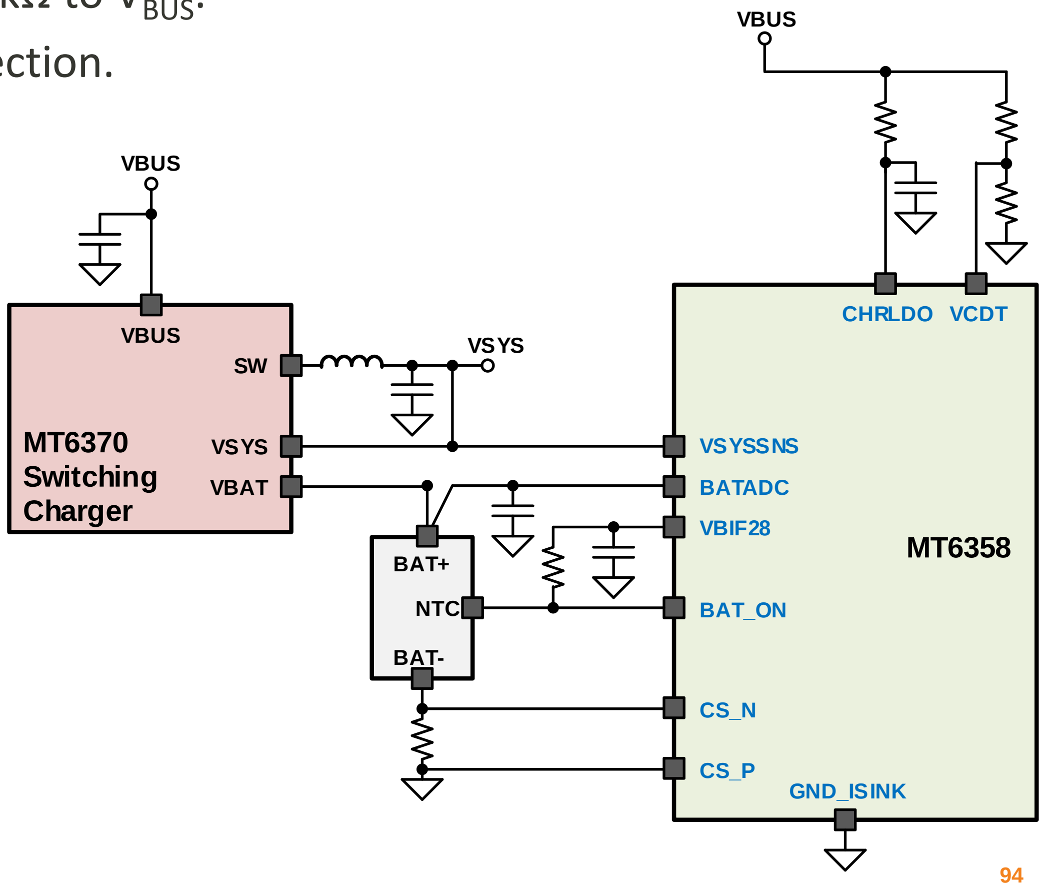
Charger

PMIC with MT6370 (w/ Power-path) Application Circuit

- If V_{BUS} up to 30V is supported, change CAP to 1uF/50V.
- VCDT for V_{BUS} detection needs ±1% resistor.
- CHRLDO connects 1.5k Ω ~ 7.5kΩ to V_{BUS}.
- CHRLDO powers for VCDT detection.
- VSYSSNS is connected to VSYS.
- VSYS MUST keep under 5V (VSYSSNS, BATADC)



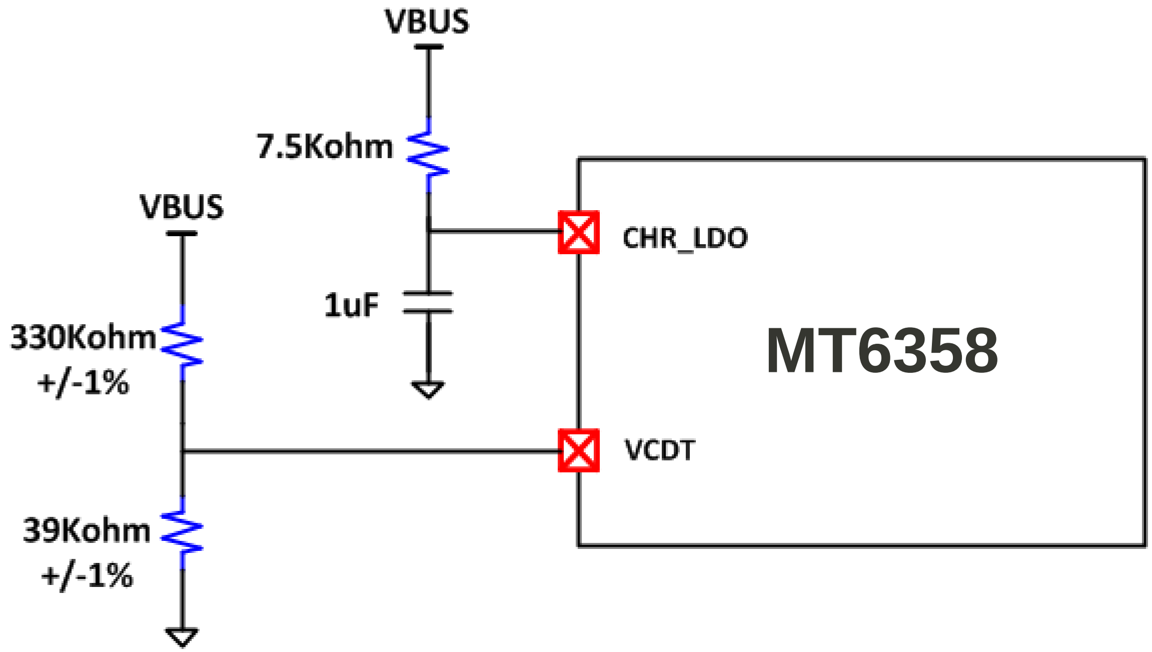
Charger Detection

Charger Detection

- **Feature**
  - Maximum input voltage up to 30V
    - (30V is system endurable voltage , not charge-able voltage)
  - VBUS plug-in/out detection
  - VBUS OVP detection

Chip / Feature	MT6358
Maximum charger input voltage	30V
VBUS rising	4.3V(default)
VBUS falling	3.9V(default)
VBUS OVP	10.5V(default)

Charger Detect Application Circuit



**Latest schematic please refer to reference design.

Charger OVP

- Charger over voltage protection HW default is enable.
  After power on, SW can configure “VCDT_HV_VTH”

Min(V)	Typical(V)	Max(V)
-6%	6	+6%
	6.5	
	7	
	7.5	
	8.5	
	9.5	
	10.5	
	11.5	
	12.5	
	14	

— HW default voltage

Charger UVLO (Rising/Falling)

- Charger UVLO detection HW default is enable.
  After power on, SW can configure "VCDT_LV_VTH"

<table>
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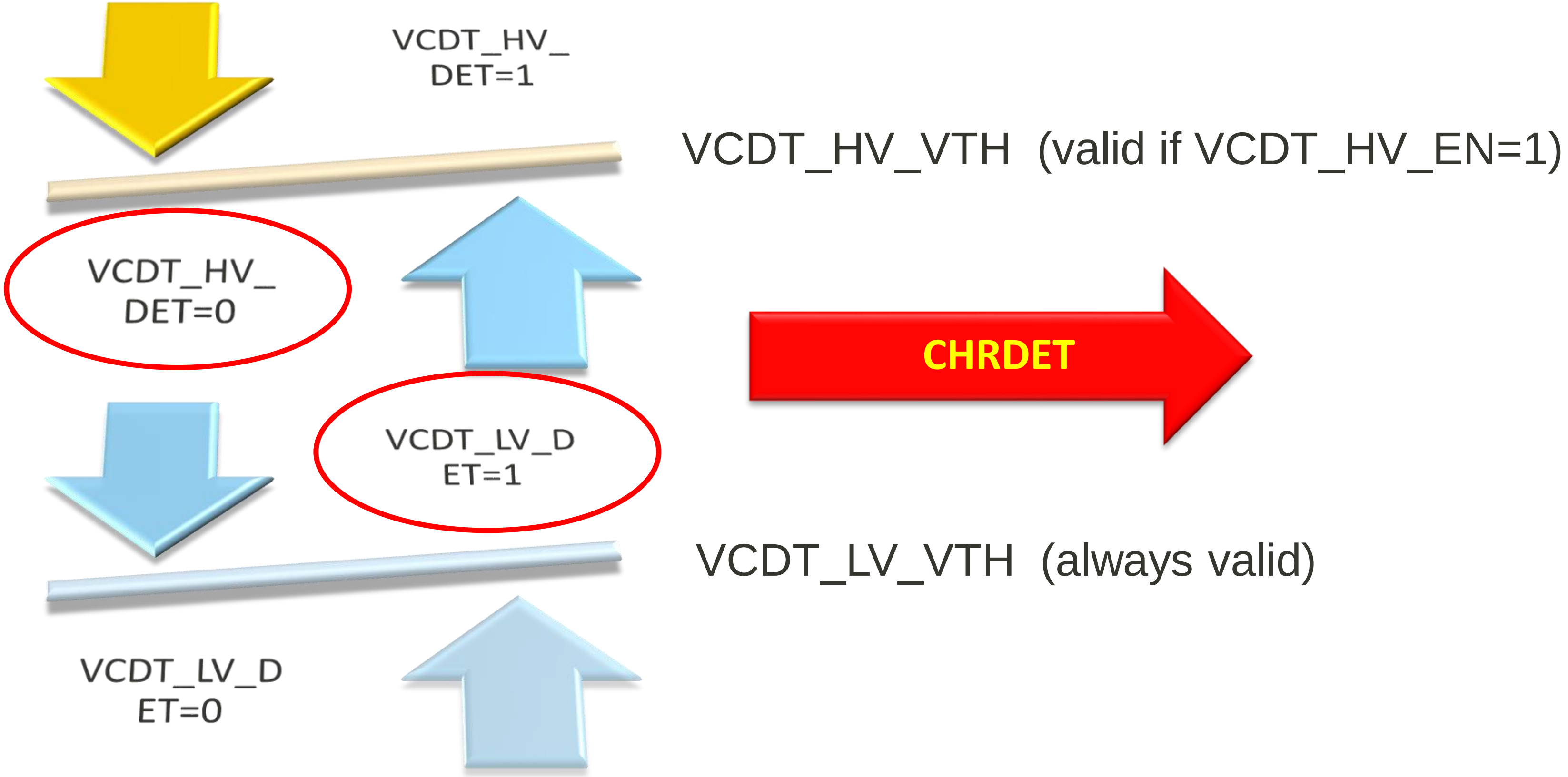
<tr><td rowspan="3">-6%</td><td>3</td><td rowspan="3">6%</td></tr>
<tr><td>3.1</td></tr>
<tr><td>3.7</td></tr>
<tr><td rowspan="2">-3%</td><td>4.3 (default)</td><td rowspan="2">3%</td></tr>
<tr><td>4.4</td></tr>
<tr><td>-6%</td><td>4.45</td><td>6%</td></tr>
</table>

<table>
<tr><th colspan="3">UVLO_Falling</th></tr>
<tr><td rowspan="12">-6%</td><td>2.8</td><td rowspan="12">6%</td></tr>
<tr><td>2.9</td></tr>
<tr><td>3</td></tr>
<tr><td>3.1</td></tr>
<tr><td>3.2</td></tr>
<tr><td>3.3</td></tr>
<tr><td>3.4</td></tr>
<tr><td>3.5</td></tr>
<tr><td>3.6</td></tr>
<tr><td>3.7</td></tr>
<tr><td>3.8</td></tr>
<tr><td>3.9 (default)</td></tr>
</table>

Charger Detect



USB-IF B.C. v1.2: Charging Port Detection

USB IF B.C. v1.2 charging port			
Define items	DCP Dedicated Charger	CDP Charging Host	SDP Standard Host
Output voltage	DC: 4.75 ~ 5.25V		
Output current	≤ 1.5A	0.5A ~ 1.5A	< 0.5A
DP/DM	DP & DM short together	DP & DM 15KΩ to GND	DP & DM 15KΩ to GND

SPI

SPI Layout Guide

- All traces of PMIC SPI bus should be well-shielded by nearby ground traces in the same layer, and surrounded by ground traces in n-1 and n+1 layers, and closed to each others.

- All traces of SPI bus should be far away from noisy sources, such as VBUS (plug-in spike), Buck switching node..etc.

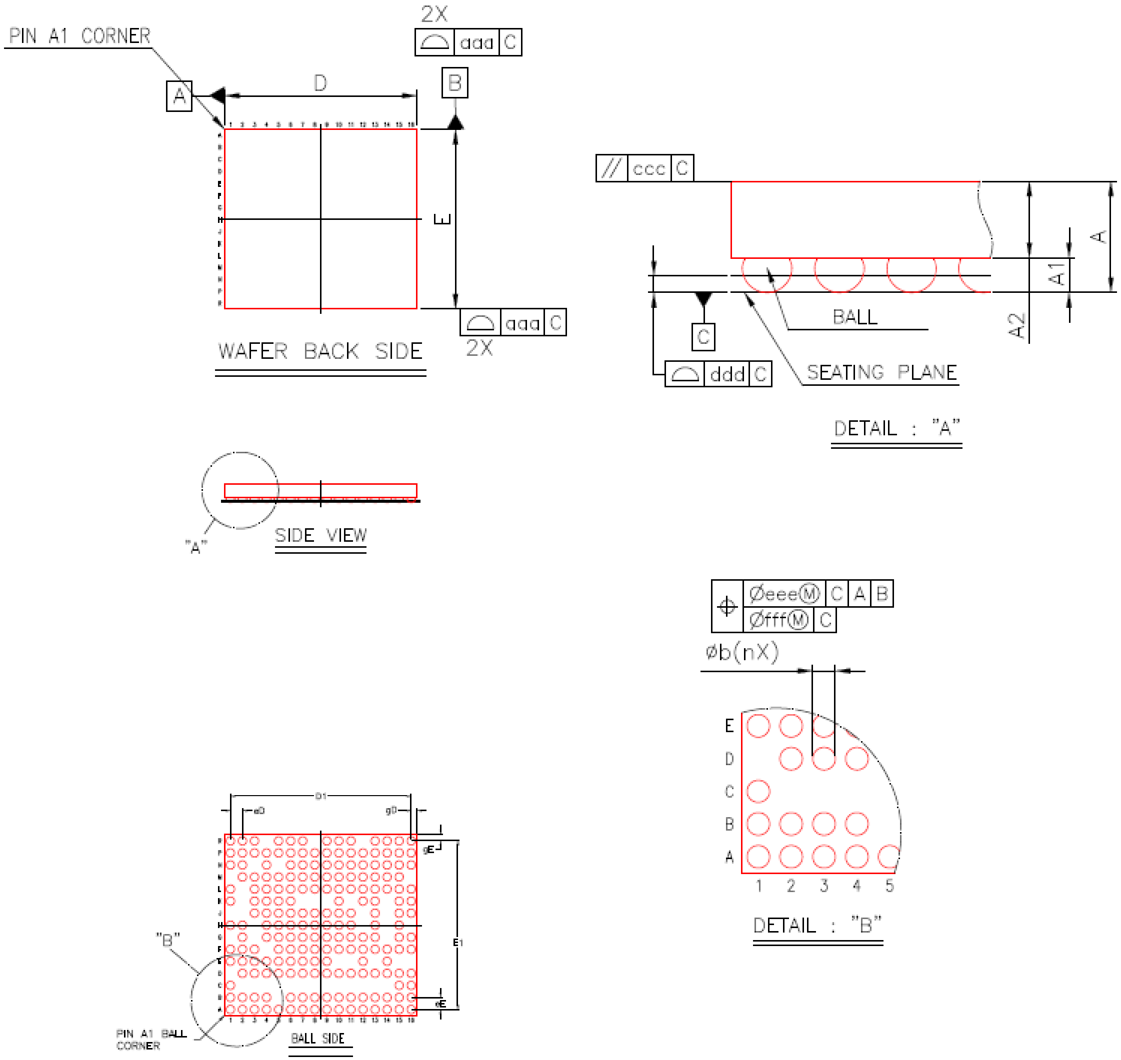
- The max. length of SPI bus between SOC and MT6358 should be shorter than 6 inches (consider 6 inches = 1ns).

Content

- MT6358 Introduction
- Function Description
- Reference Design
- Function Block Notice
- **PCB Layout Guideline**

MT6358
PCB LAYOUT GUIDELINE

Package Outline of MT6358



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MIFO WLCSP		
Body Size	X	D	6.30	6.40	6.50
	Y	E	5.90	6.00	6.10
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Total Thickness		A	0.580	0.620	0.660
Ball Stand Off		A1	0.170	0.195	0.220
Body Thickness		A2	0.400	0.425	0.450
Ball Width		b	0.245	0.275	0.305
Ball Diameter			0.250		
Body Edge Tolerance		aaa	0.10		
Body Flatness		ccc	0.10		
Coplanarity		ddd	0.05		
Ball Offset (Package)		eee	0.10		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	194		
Edge Ball Center to Center	X	D1	6.00		
	Y	E1	5.60		
Edge Ball Center to Body Edge	X	gD	0.20		
	Y	gE	0.20		

MT6358 Ball Map

194	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	VS1	GND_VS1	VPA	VSYS_VPA	VSYS_VPROC11	VPROC11	GND_VPROC11	VPROC12	VSYS_VPROC12	VSYS_VGPU	VGPU	GND_VCORE	VCORE	VSYS_VCORE	NC	A
B	VSYS_VS1	VS1	GND_VS1	GND_VPA		VSYS_VPROC11	VPROC11	GND_VPROC11	VPROC12	VSYS_VPROC12	VSYS_VGPU	VGPU	GND_VCORE	VCORE	VSYS_VCORE	GND_VCORE_FB	B
C	VSYS_VS1														GND_VGPU_FB	VCORE_FB	C
D		PWRKEY	EXT_PMIC_EN1	RESETB	VPA_FB	VPROC11_FB	GND_VPROC11_FB	GND_VPROC12	GND_VPROC12	GND_VPROC12_FB	VDRAM1_FB	GND_VGPU	GND_VGPU	VGPU_FB	VMODEM_FB	VS2_FB	D
E	GND_SMPS	VSYS_SMPS	VEFUSE	VS1_LDO1	EXT_PMIC_EN2	VCAMIO	VS1_FB	PMU_TESTMODE	VPROC12_FB			GND_VDRAM1_FB		GND_VMODEM_FB			E
F	AU_V18N	FLYN	VIO18		VRF18	VCN18	D_GND	D_GND	D_GND	RTC32K_1V8_0	SPI_CLK	WDTRSTB_IN	SPI_CSN	VSYS_VMODEM	VMODEM	VMODEM	F
G		FLYP		AU_HPR	AU_LOLP	AU_LOLN	D_GND	D_GND	D_GND	SPI_MISO	SPI_MOSI	RTC32K_1V8_1	HOMEKEY		GND_VMODEM	GND_VMODEM	G
H	AVSS18_AUD	AVDD18_AUD		AU_HPL	AU_REFN	AU_HSN	D_GND	D_GND	D_GND	AUD_CLK_MISO	AUD_DAT_MISO1		SCP_VREQ_VAO		GND_VDRAM1		H
J			AVDD28_AUD	HP_EINT	AVSS28_AUD	AU_HSP	SRCLKEN_IN1	DVDD18_DIG	AUD_DAT_MOSI0	AUD_SYNC_MISO	AUD_DAT_MISO0		SD_CARD_DET_N		VDRAM1	VSYS_VDRAM1	J
K	AU_VIN0_P		AU_VIN2_N	AU_VIN2_P	AU_MICBIAS0	ACCDET				AUD_SYNC_MOSI		VCDT	CHRLDO		VSYS_VS2	VSYS_VS2	K
L	AU_VIN0_N		AU_VIN1_N	AU_VIN1_P	AU_MICBIAS1	FSOURCE	SRCLKEN_IN0	DVSS18_IO	DVDD18_IO	AUD_DAT_MOSI1	AUD_CLK_MOSI	BATON	BATADC	GND_VS2	VS2	VS2	L
M		AUXADC_VIN	AVDD18_AUXADC	AVSS18_AUXADC	CS_N	VAUX18	RTC32K_2V8	VRTC28	VBIF28	VCAMA1	VSYSSNS	VREF	UVLO_VTH	VS2_LDO4	VCAMD		M
N	XTAL1	AVSS22_XO_ISO		XO_NFC		CS_P	VSIM1	VUSB	VIO28	VCAMA2	VSYS_LDO3	VCN33	GND_VREF	VS2_LDO2	VRF12	VA12	N
P	XTAL2	AVSS22_XO	XO_WCN	XO_SOC	XO_EXT	VXO22	VSYS_LDO1	VLDO28	VSYS_LDO2	VSIM2	VIBR	VSRAM_PROC11	VS2_LDO3	VSRAM_OTHERS	VDRAM2	VRF12_S	P
R	NC	AVSS22_XOBUF	XO_CEL		VAUD28	VCAMA1	VFE28		VMC	VMCH	VEMC		VSRAM_PROC12	VSRAM_GPU	VS2_LDO1	NC	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

(green)	Power Input
(purple)	Buck Output
(orange)	LDO Input
(pink)	LDO Output
(gray)	GND
(cyan)	Audio Input/Output
(blue)	AUX_ADC
(dark purple)	DCXO
(magenta)	RTC
(red-pink)	Charge

MT6358 Power Input (1/2)

VSYS Input

- Routing from 22uF VSYS capacitor uses start topology to connect to each device.
  1. **VSYS** input for BUCK. (Fig. 2)
  2. **VSYS** input for LDO. (Fig. 2)
- Follow the trace width rule in. (Fig. 3)
- All the decoupling capacitors should be placed near MT6358. The priority is buck capacitor then decoupling capacitor of LDO. (Fig.1)

Fig. 3

IC Ball Name	IMAX(mA)
VSYS_SMPS	10
VSYS_VPROC11	4600
VSYS_VPROC12	3190
VSYS_VCORE	4600
VSYS_VMODEM	3250
VSYS_VS1	2000
VSYS_VS2	2000
VSYS_VPA	1000
VSYS_GPU	3310
VSYS_VDRAM1	2000
VSYS_LDO1	2000
VSYS_LDO2	2000
VSYS_LDO3	2000

Fig. 1

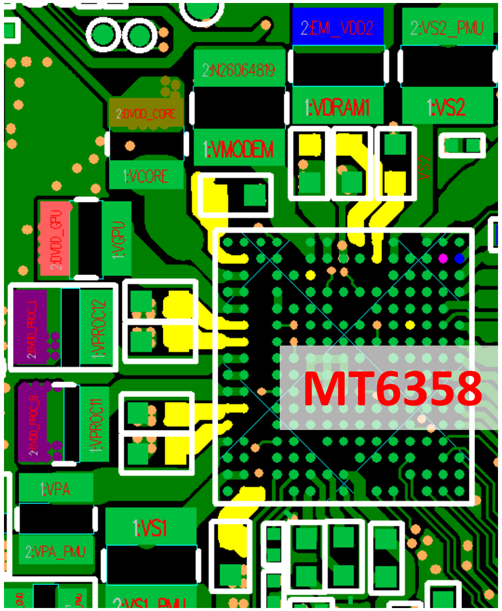
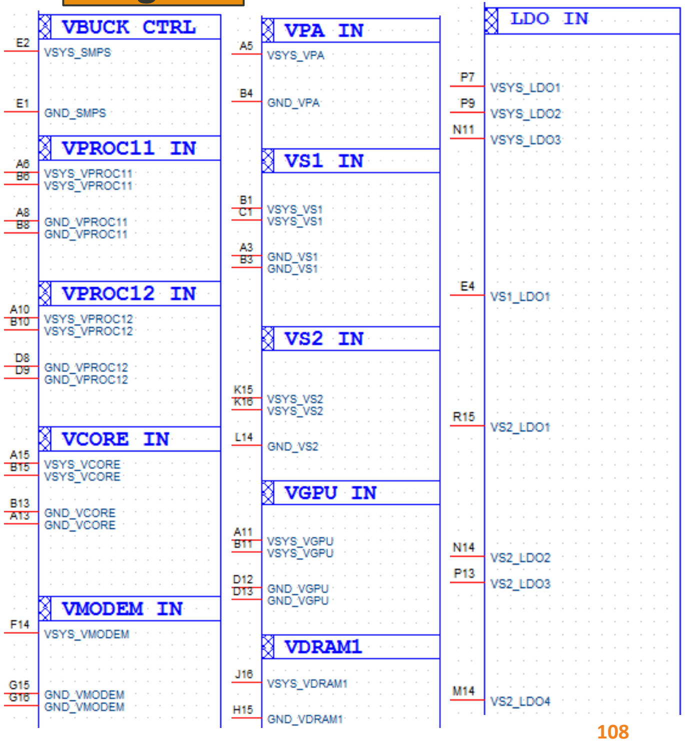


Fig. 2



MT6358 Power Input (2/2)

- **Layout method of MT6358 power Input for Buck GND**
  - Buck GND balls are connected to buck capacitors close to pin with plane or trace (Trace Width > **8mil * N (ball number) + M (ball pitch)**). (Fig.1~2)
  - Buck GND balls should be connected to buck capacitors first and isolated from the nearby GND trace and plane then connected to main GND at L3 (Fig.1~2).

Fig.1

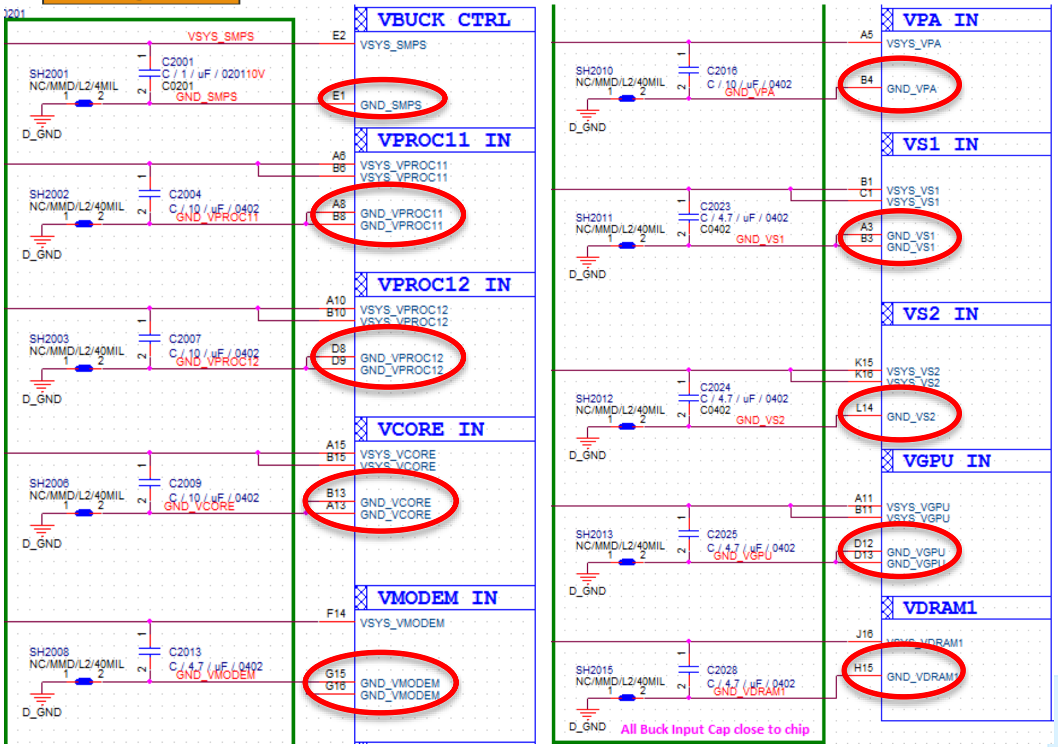
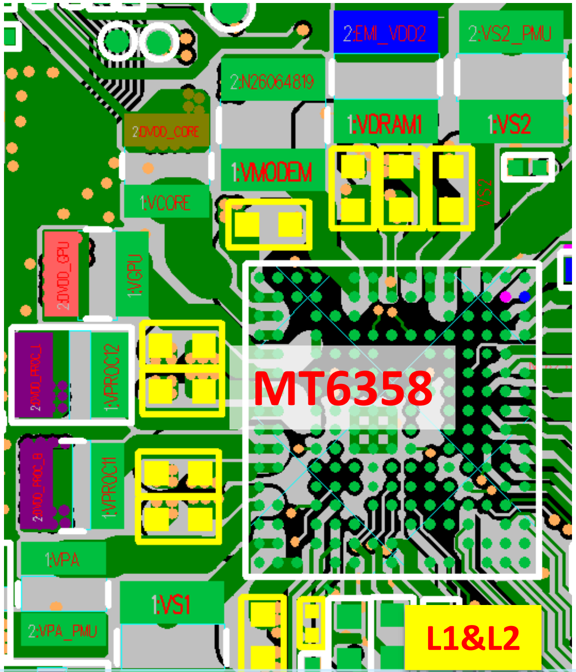


Fig.2



Layer 2: BUCK GND is isolated from nearby GND trace and plane.

MT6358 Buck Output (1/2)

- The buck inductors should be placed near MT6358. (Fig.1)
- The output current is shown in Fig.2.

Fig.1

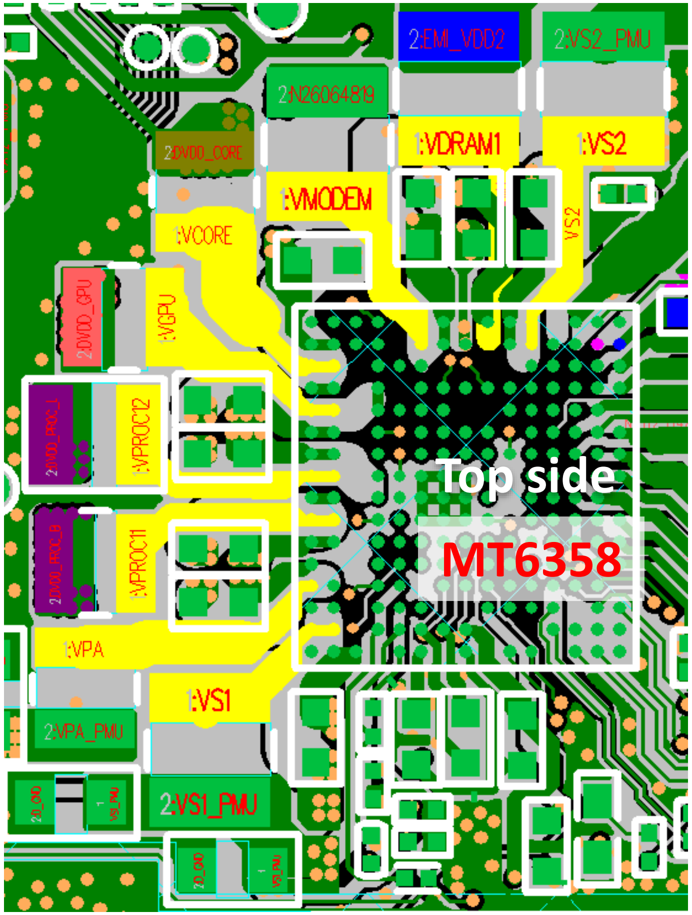
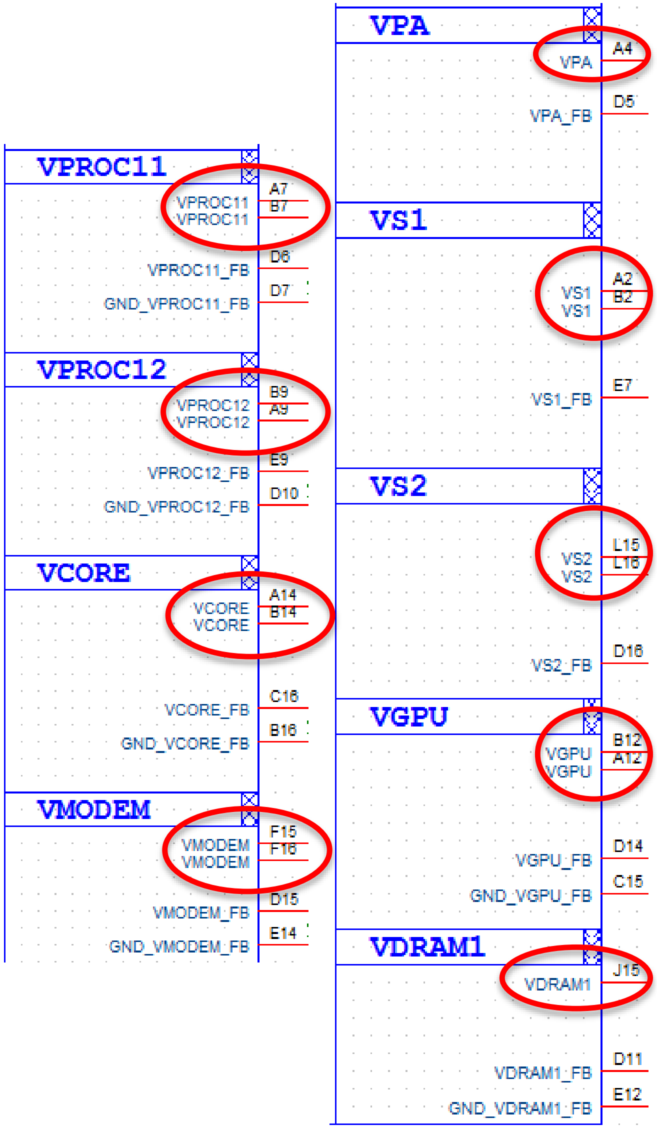


Fig.2

Regulator	Output Current(mA)
VS1	2000
VS2	2000
VDRAM1	2000
VMODEM	3250
VPA	1000
VPROC11	4600
VPROC12	3190
VCORE	4600
VGPU	3310



MT6358 Buck Output (2/2)

- Those signals are differential pairs and should be shielded by GND and far away from noise signals (Fig.1 ~ Fig.2).
    1. VMODEM_FB/GND_VMODEM_FB
    2. VPROC11_FB/GND_VPROC11_FB
    3. VPROC12_FB/GND_VPROC12_FB
    4. VCORE_FB/GND_VCORE_FB
    5. VGPU_FB/GND_VGPU_FB
    6. VDRAM1_FB/GND_VDRAM1_FB
    7. VS1_FB, VS2_FB, VPA_FB

Fig. 1

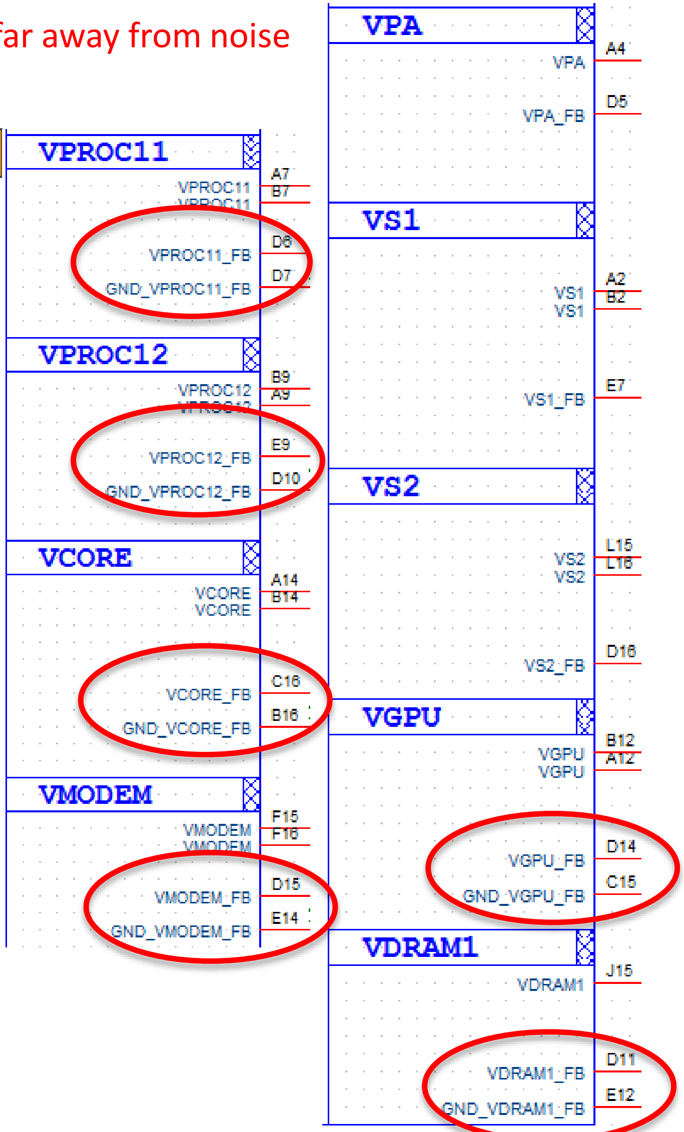
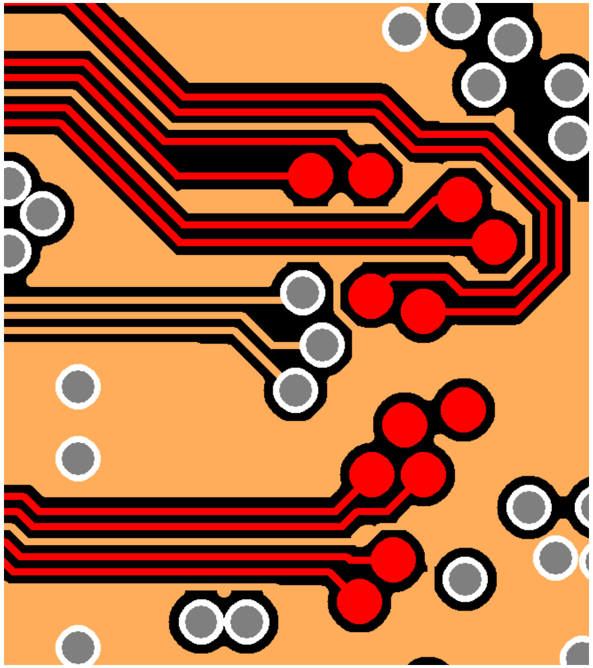
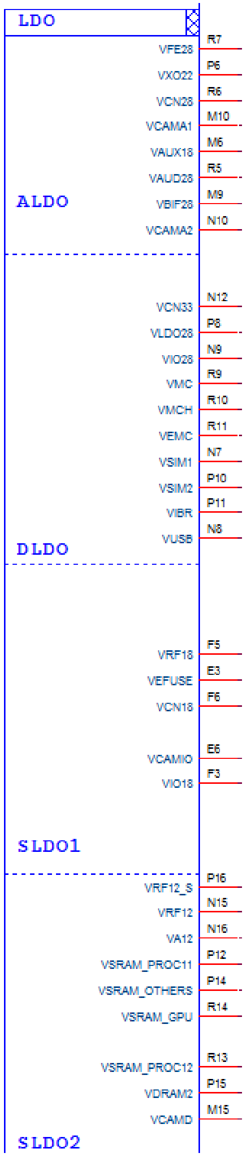


Fig. 2



MT6358 LDO Output (1/2)

- See table. for the suggested LDO output layout.

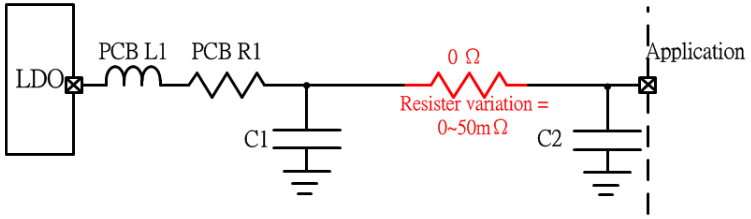


1. Trace width≧6mil
2. Value and placement of Capacitor please refer design notice

Ball name	Imax	Trace Length	Trace Width	Rpcb H=50um, 1/3 oz	PCB drop voltage
VFE28	50mA	2500mil	6mil	670mΩ	34mV
VXO22	50mA	2500mil	6mil	670mΩ	34mV
VCN28	50mA	2500mil	6mil	670mΩ	34mV
VCAMA1	200mA	2500mil	6mil	670mΩ	134mV
VAUX18	50mA	2500mil	6mil	670mΩ	34mV
VAUD28	50mA	2500mil	6mil	670mΩ	34mV
VBIF28	50mA	2500mil	6mil	670mΩ	34mV
VCAMA2	200mA	2500mil	6mil	670mΩ	134mV
VCN33	800mA	1000mil	20mil	80mΩ	64mV
VLDO28	400mA	2500mil	10mil	402mΩ	161mV
VIO28	200mA	2500mil	6mil	670mΩ	134mV
VMC	200mA	2500mil	6mil	670mΩ	134mV
VMCH	800mA	1000mil	20mil	80mΩ	64mV
VEMC	800mA	1000mil	20mil	80mΩ	64mV
VSIM1	200mA	2500mil	6mil	670mΩ	134mV
VSIM2	200mA	2500mil	6mil	670mΩ	134mV
VIBR	200mA	2500mil	6mil	670mΩ	134mV
VUSB	200mA	2500mil	6mil	670mΩ	134mV
VRF18	450mA	1000mil	14mil	115mΩ	52mV
VEFUSE	300mA	2500mil	8mil	503mΩ	151mV
VCN18	300mA	2500mil	8mil	503mΩ	151mV
VCAMIO	300mA	2500mil	8mil	503mΩ	151mV
VIO18	700mA	1000mil	16mil	101mΩ	70mV
VRF12_S	0mA	x	x	x	x
VRF12	800mA	1000mil	20mil	80mΩ	64mV
VA12	300mA	2500mil	8mil	503mΩ	151mV
VSRAM_PROC11	600mA	1000mil	16mil	101mΩ	60mV
VSRAM_OTHERS	600mA	1000mil	16mil	101mΩ	60mV
VSRAM_GPU	600mA	1000mil	16mil	101mΩ	60mV
VSRAM_PROC12	600mA	1000mil	16mil	101mΩ	60mV
VDRAM2	600mA	1000mil	16mil	101mΩ	60mV
VCAMD	600mA	2500mil	16mil	251mΩ	151mV

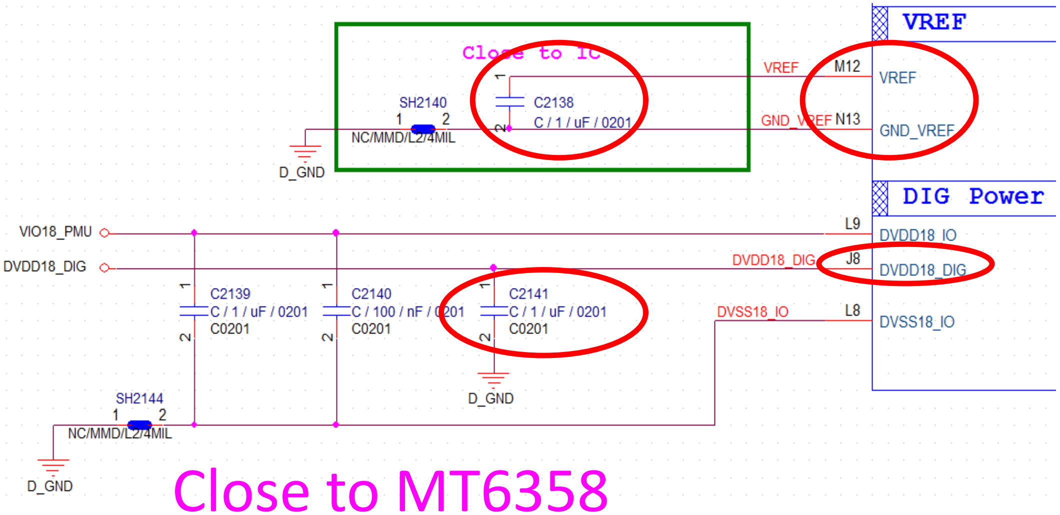
- VRF18/VRF12/VRF12_S:
  - **Traces should be in inner layer or under shielding case.**
- VRF12_S:
  - **For MT6177, VRF12_S should connect to ball VRF12**
- Trace width/length can adjust by application Imax

If trace is series 0Ω resister, 0Ω resister is having 0~50mΩ variation. It would be drop voltage.

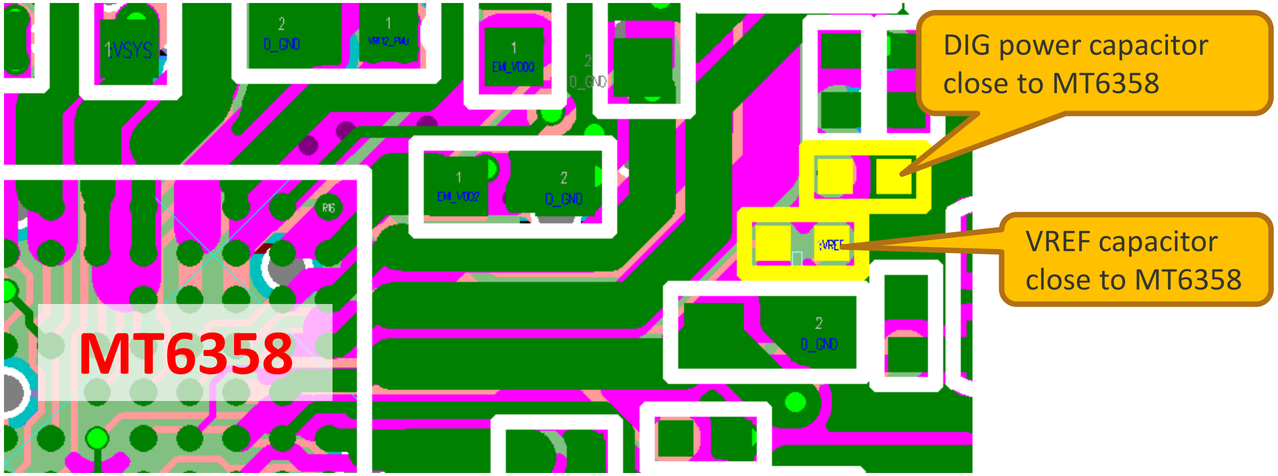


MT6358 LDO Output (2/2)

- VREF capacitor should be placed near M12/N13 pin.
- DVDD18_DIG capacitor should be placed near J8 pin.



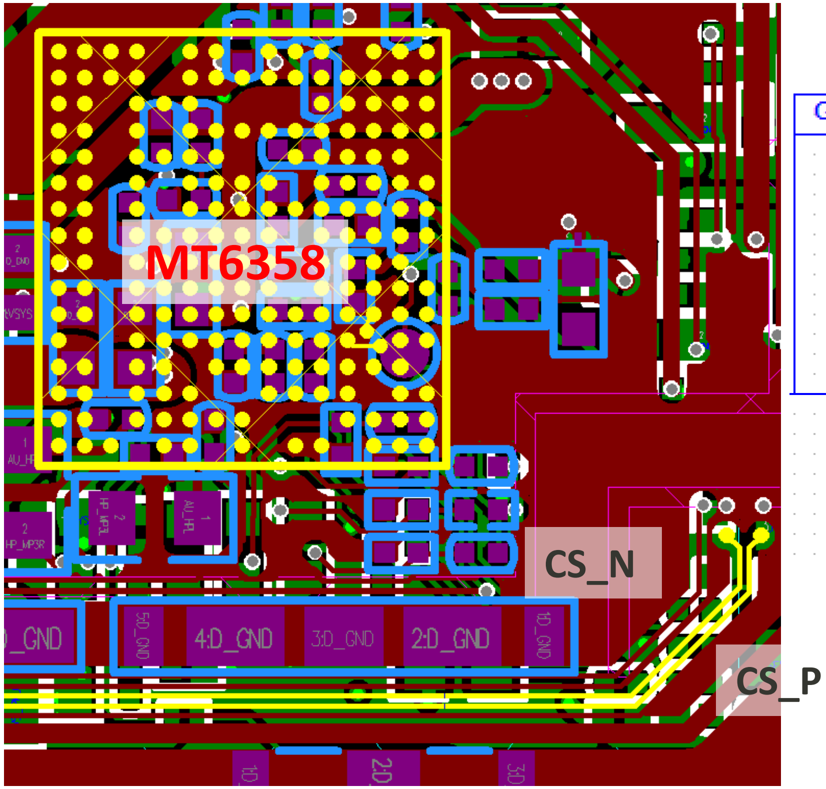
Close to MT6358

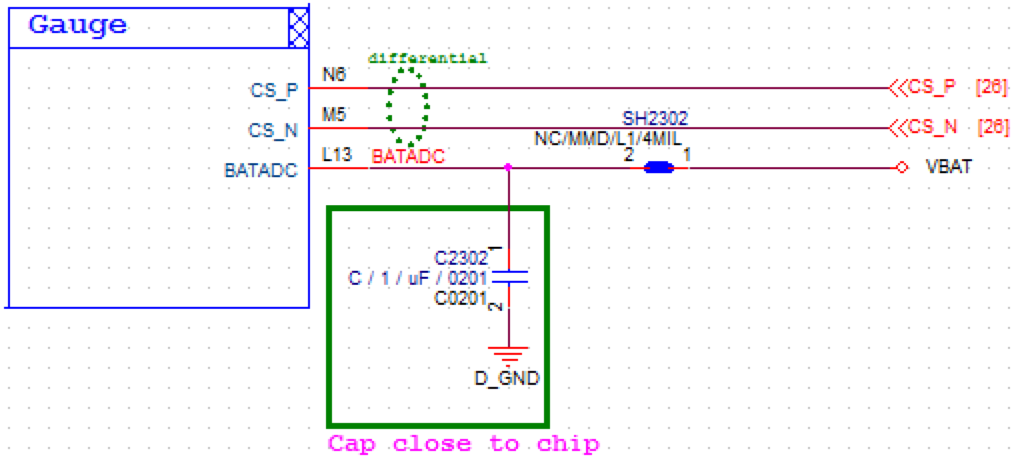


Others for MT6358

Gauge-

- CS_N/CS_P (ball: M5/N6) should be routed as differential pairs and far away from noise signals.





MT6358 Audio PCB Layout Guide

- MT6358 Audio PCB Layout Guide

  Please refer “ MT6771 Design Notice “

MT6358 AUXADC / DCXO PCB Layout Guide

- MT6358 AUXADC /DCXO PCB Layout Guide

  Please refer “ MT6771_MT6358 Co-TMS Design Notice “

How to Connection for Unused Pin

Unused Part	Pin Name	Description	Pin Connection if not used
Interface	EXT_PMIC_EN1	Ext chip enable pin1	Floating
	EXT_PMIC_EN2	Ext chip enable pin2	Floating
	HOMEKEY	HOMEKEY button with default long press function	Short to GND
		HOMEKEY button without default long press function	Floating
PCHR	BATON	Battery NTC pin for battery and its temperature sensing	Pull-Low 10KΩ to GND
Gauge	BATADC	Fuel gauge ADC input pin for monitoring battery voltage	VBAT
	CS_N	Fuel gauge ADC input pin	GND
	CS_P	Fuel gauge ADC input pin	GND

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